

【Instruction】

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【Instruction】

Chapter 1 PLC Ladder Diagram and the Coding Rules of Mnemonic

In this chapter, we would like to introduce you the basic principles of ladder diagram, in addition, the coding rules of Mnemonic will be introduced as well, it's essential for the user who use FP-08 as a programming tool. If you are familiar with PLC Ladder Diagram and mnemonic coding rules, you may skip this chapter.

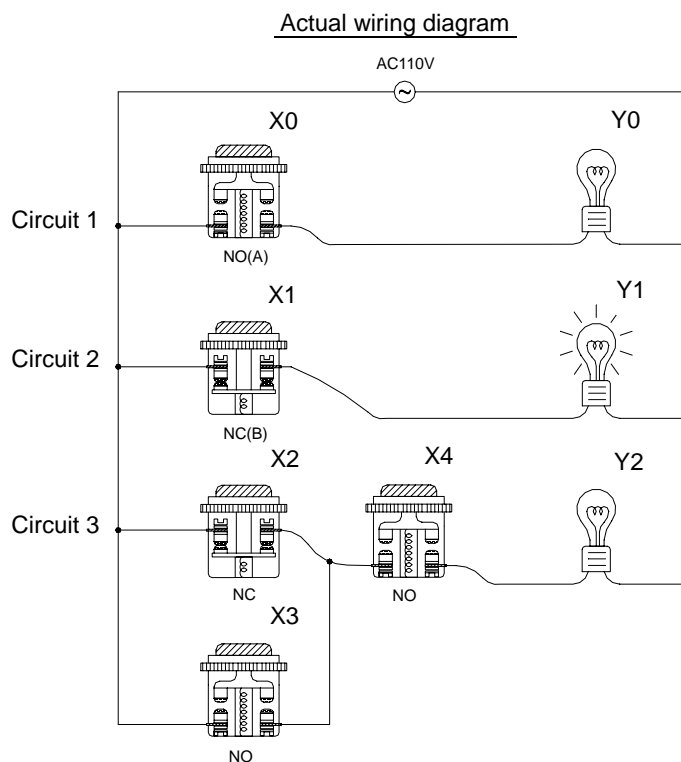
1.1 The Operation Principle of Ladder Diagram

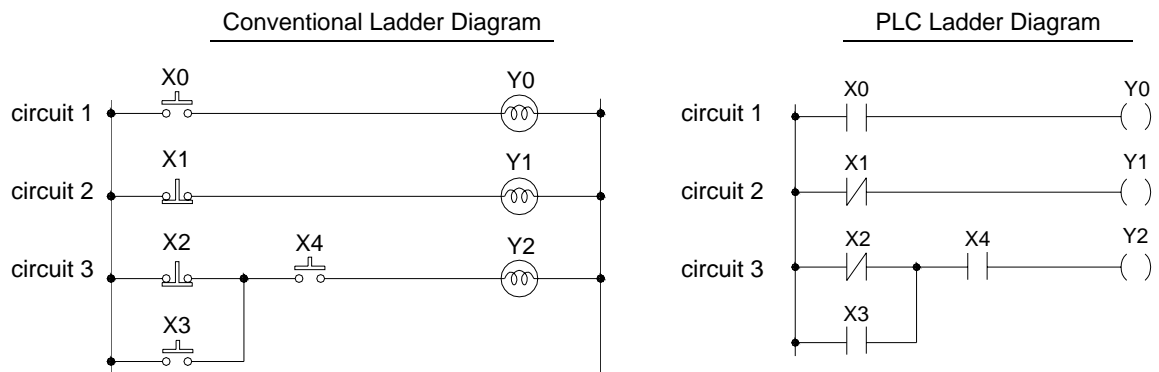
Ladder Diagram is a type of graphic language for automatic control systems it had been used for a long period since World War II. Until today, it is the oldest and most popular language for automatic control systems. Originally there are only few basic elements available such as A-contact (Normally ON), B contact (Normally OFF), output Coil, Timers and Counters. Not until the appearance of microprocessor based PLC, more elements for Ladder Diagram, such as differential contact, retentive coil (refer to page 1-6) and other instructions that a conventional system cannot provide, became available.

The basic operation principle for both conventional and PLC Ladder Diagram is the same. The main difference between the two systems is that the appearance of the symbols for conventional Ladder Diagram are more closer to the real devices, while for PLC system, symbols are simplified for computer display. There are two types of logic system available for Ladder Diagram logic, namely combination logic and sequential logic. Detailed explanations for these two logics are discussed below.

1.1.1 Combination Logic

Combination logic of the Ladder Diagram is a circuit that combines one or more input elements in series or parallel and then send the results to the output elements, such as Coils, Timers/Counters, and other application instructions.



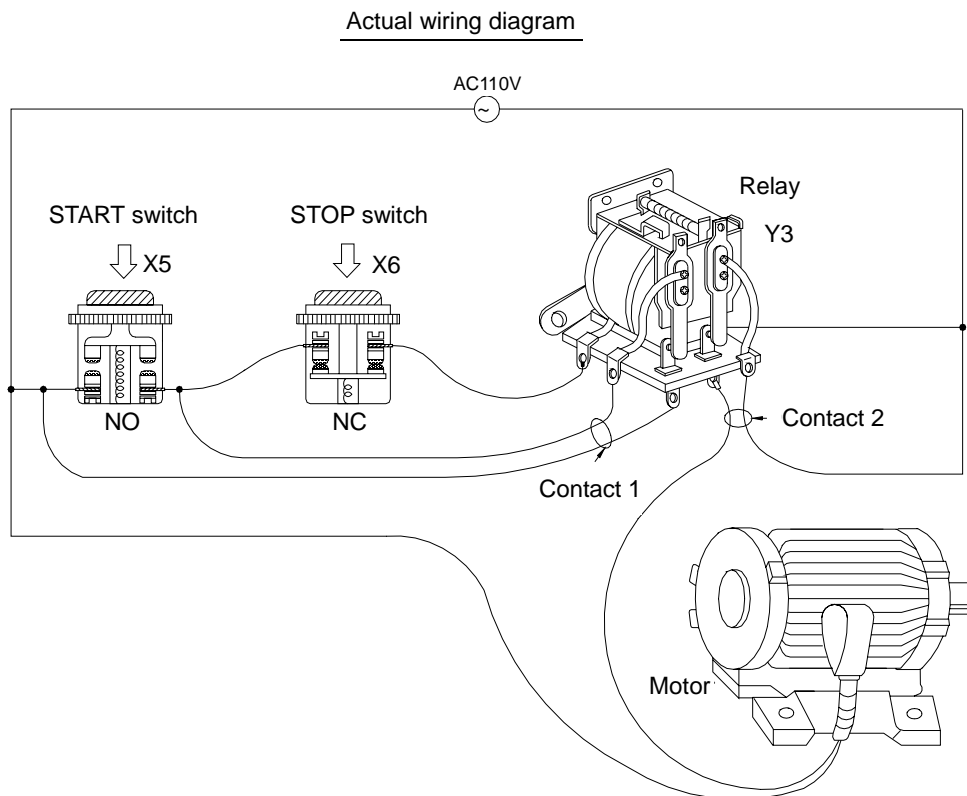


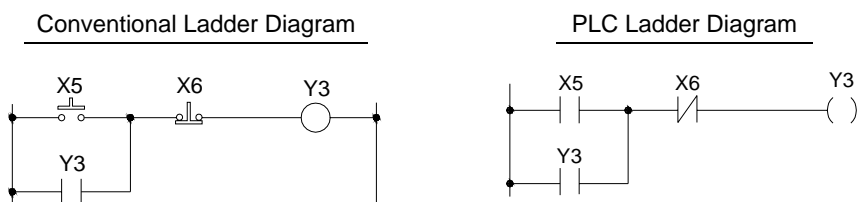
The above example illustrated the combination logic using the actual wiring diagram, conventional Ladder Diagram, and PLC Ladder Diagram. Circuit 1 uses a NO (Normally Open) switch that is also called "A" switch or contact. Under normal condition (switch is not pressed), the switch contact is at OFF state and the light is off. If the switch is pressed, the contact status turns ON and the light is on. In contrast, circuit 2 uses a NC (Normally Close) switch that is also called "B" switch or contact. Under normal condition, the switch contact is at ON state and the light is on. If the switch is pressed, the contact status turns OFF and the light also turns off.

Circuit 3 contains more than one input element. Output Y2 light will turn on under the condition when X2 is closed or X3 switches to ON, and X4 must switch ON too.

1.1.2 Sequential Logic

The sequential logic is a circuit with feedback control; that is, the output of the circuit will be feedback as an input to the same circuit. The output result remains in the same state even if the input condition changes to the original position. This process can be best explained by the ON/OFF circuit of a latched motor driver as shown in below.





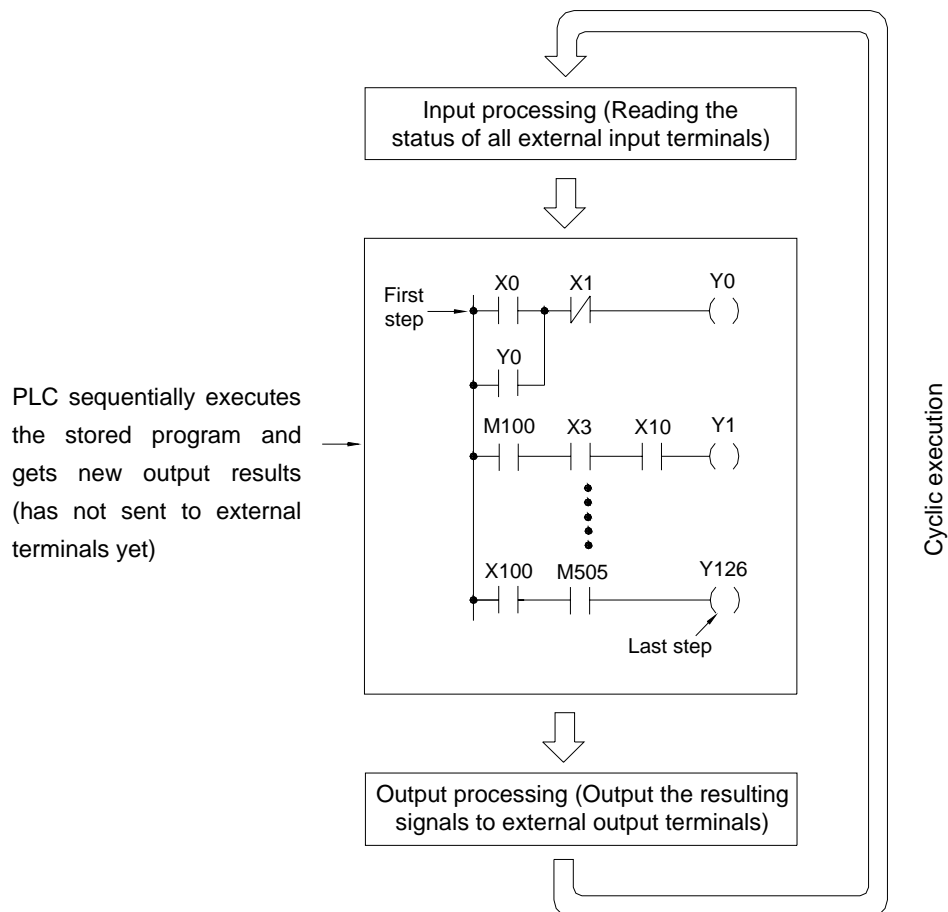
When we first connect this circuit to the power source, X6 switch is ON but X5 switch is OFF, therefore the relay Y3 is OFF. The relay output contacts 1 and 2 are OFF because they belong to A contact (ON when relay is ON). Motor does not run. If we press down the switch X5, the relay turns ON as well as contacts 1 and 2 are ON and the Motor starts. Once the relay turns ON, if we release the X5 switch (turns OFF), relay can retain its state with the feedback support from contact 1 and it is called Latch Circuit. The following table shows the switching process of the example we have discussed above.

	X5 switch (NO)	X6 switch (NC)	Motor (Relay) status
①	Released	Released	OFF
↓			
②	Pressed	Released	ON
↓			
③	Released	Released	ON
↓			
④	Released	Pressed	OFF
↓			
⑤	Released	Released	OFF

From the above table we can see that under different stages of sequence, the results can be different even the input statuses are the same. For example, let's take a look at stage ① and stage ③, X5 and X6 switches are both released, but the Motor is ON (running) at stage ③ and is OFF (stopped) at stage ①. This sequential control with the feedback of the output to the input is a unique characteristic of Ladder Diagram circuit. Sometimes we call the Ladder Diagram a "Sequential Control Circuit" and the PLC a "Sequencer". In this section, we only use the A/B contacts and output coils as the example. For more details on sequential instructions please refer to chapter 5 - "Introduction to Sequential Instructions."

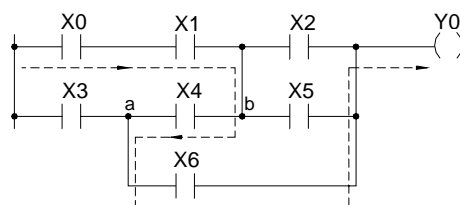
1.2 Differences Between Conventional and PLC Ladder Diagram

Although the basic operation principle for both conventional and PLC Ladder Diagram are the same, but in reality, PLC uses the CPU to emulate the conventional Ladder Diagram operations; that is, PLC uses scanning method to monitor the statuses of input elements and output coils, then uses the Ladder Diagram program to emulate the results which are the same as the results produced by the conventional Ladder Diagram logic operations. There is only one CPU, so the PLC has to sequentially examine and execute the program from its first step to the last step, then returns to the first step again and repeats the operation (cyclic execution). The duration of a single cycle of this operation is called the scan time. The scan time varies with the program size. If the scan time is too long, then input and output delay will occur. Longer delay time may cause big problems in controlling fast response systems. At this time, PLCs with short scan time are required. Therefore, scan time is an important specification for PLCs. Due to the advance in microcomputer and ASIC technologies nowadays the scan speed has been enhanced a great deal. A typical FB_E-PLC takes approximately 0.33 ms for 1K steps of contact. The following diagram illustrates the scanning process of a PLC Ladder Diagram.

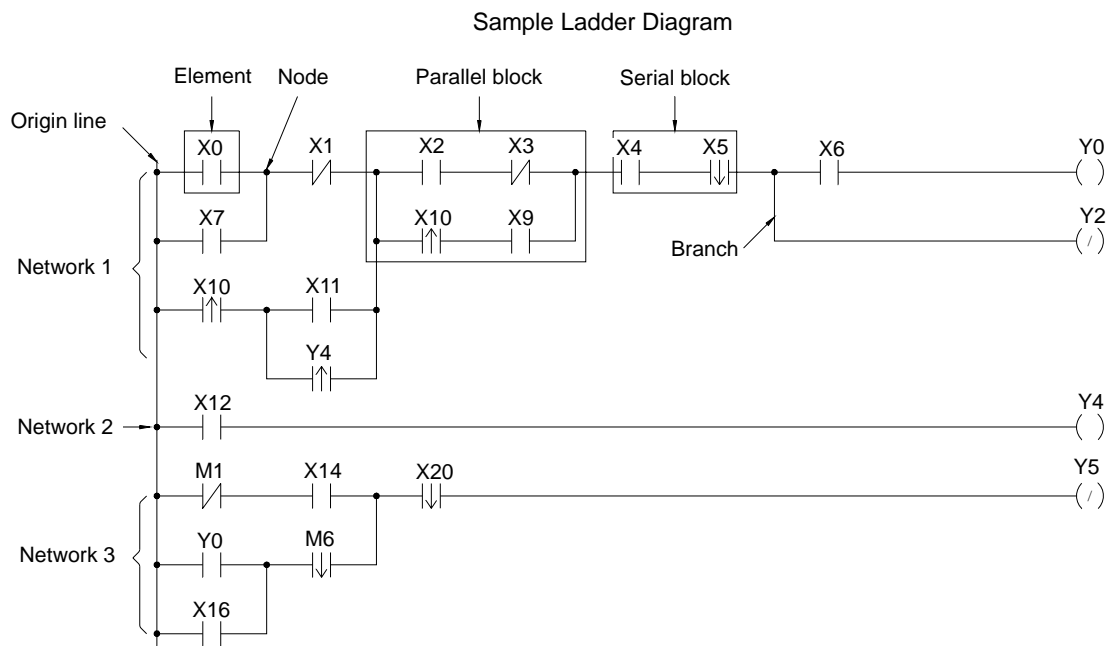


Besides the time scan difference mentioned above, the other difference between the conventional and PLC Ladder Diagram is “Reverse flow” characteristic. As shown in the diagram below, if X0, X1, X4 and X6 are ON, and the remaining elements are OFF. In a conventional Ladder Diagram circuit, a reverse flow route for output Y0 can be defined by the dashed line and Y0 will be ON. While for PLC, Y0 is OFF because the PLC Ladder Diagram scans from left to right, if X3 is off then CPU believes node “a” is OFF, although X4 and node “b” are all ON, since the PLC scan reaches X3 first. In other words, the PLC ladder can only allow left to right signal flow while conventional ladder can flow bi-directional.

Reverse flow of conventional Ladder diagram



1.3 Ladder Diagram Structure and Terminology



(Remark : The maximum size of FBs-PLC network is 16 rows × 22 columns)

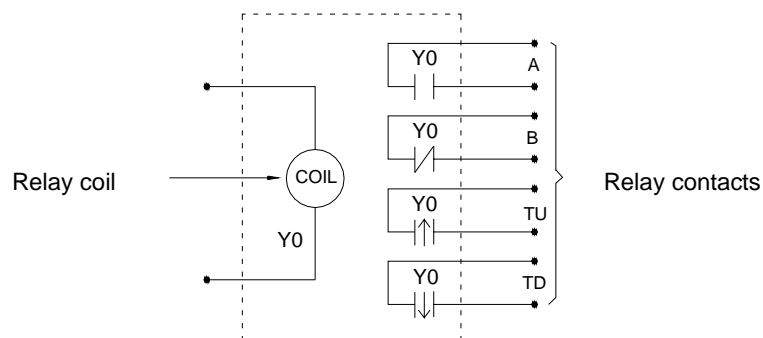
As shown above, the Ladder Diagram can be divided into many small cells. There are total 88 cells (8 rows X 11 columns) for this example Ladder Diagram. One cell can accommodate one element. A completed Ladder Diagram can be formed by connecting all the cells together according to the specific requirements. The terminologies related to Ladder Diagram are illustrated below.

① Contact

Contact is an element with open or short status. One kind of contact is called "Input contact"(reference number prefix with X) and its status reference from the external signals (the input signal comes from the input terminal block). Another one is called "Relay contact" and its status reflects the status of relay coil (please refer to ②). The relation between the reference number and the contact status depends on the contact type. The contact elements provided by FB series PLC include: A contact, B contact, up/down differential (TU/TD) contacts and Open/Short contacts. Please refer to ④ for more details.

② Relay

Same as the conventional relay, it consists of a Coil and a Contact as shown in the diagram below.

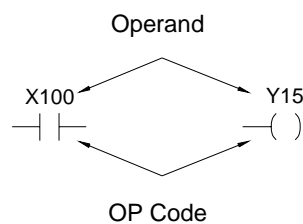


We must energize the coil of relay first (using OUT instruction) in order to turn on the relay. After the coil is energized, its contact status will be ON too. As shown in the example above, if Y0 turns ON, then the relay contact A is ON and contact B is OFF, TU contact only turns ON for one scan duration and TD contact is OFF. If Y0 turns OFF, then the relay contact A is ON and contact B is ON, TU contact is OFF and TD contact only turns ON for one scan duration (Please refer to chapter 4 “Introduction to Sequential Instructions” for operations of A,B,TU and TD contacts).

There are four types of FB-PLC relays, namely Y△△△ (output relay) , M△△△△ (internal relay) , S△△△ (step relay) and TR△△ (temporary relay) . The statuses of output relays will be sent to the output terminal block.

③ Origin-line: The starting line at the left side of the Ladder Diagram.

④ Element: Element is the basic unit of a Ladder Diagram. An element consists of two parts as shown in the diagram below. One is the element symbol which is called “OP Code” and another is the reference number part which is called “Operand”.



Element type	Symbol	Mnemonic instructions	Remark
A Contact (Normally OPEN)		(ORG 、 LD 、 AND 、 OR) □△△△△	□ can be X 、 Y 、 M 、 S 、 T 、 C (please refer to section 2.2)
B Contact (Normally CLOSE)		(ORG 、 LD 、 AND 、 OR) NOT □△△△△	
Up Differential Contact		(ORG 、 LD 、 AND 、 OR) TU □△△△△	□ can be X 、 Y 、 M 、 S
Down Differential Contact		(ORG 、 LD 、 AND 、 OR) TD □△△△△	
Open Circuit Contact		(ORG 、 LD 、 AND 、 OR) OPEN	
Short Circuit Contact		(ORG 、 LD 、 AND 、 OR) SHORT	
Output Coil		OUT □△△△△	□ can be Y 、 M 、 S
Inverse Output Coil		OUT NOT □△△△△	
Latching Output Coil	Y△△△ —(L)	OUT L Y△△△	

Remark : please refer to section 2.2 for the ranges of X 、 Y 、 M 、 S 、 T and C contacts. Please refer to section 4.2 for the characteristics of X 、 Y 、 M 、 S 、 T and C contacts.

There are three special sequential instructions, namely OUT TRn, LD TRn and FOn, which were not displayed on the Ladder Diagram. Please refer to section 1.6 “Using the Temporary Relay” and section 5.1.4 “Function Output FO”.

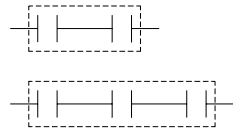
⑤ Node: The connection point between two or more elements (please refer to section 4.3)

⑥ Block: a circuit consists of two or more elements.

There are two basic types of blocks:

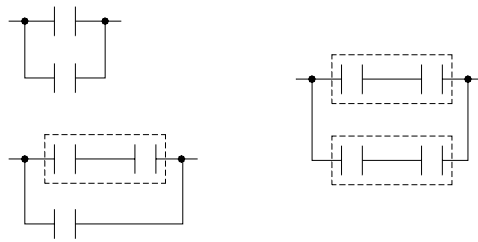
- Serial block : Two or more elements are connected in series to form a single row circuit.

Example:



- Parallel block: Parallel block is a type of a parallel closed circuit formed by connecting elements or serial blocks in parallel.

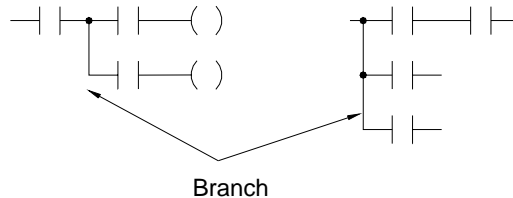
Example:



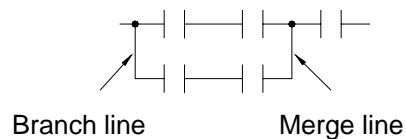
Remark: Complicated block can be formed by the combination of the single element, serial blocks and parallel blocks. When design a Ladder Diagram with mnemonic entry, it is necessary to break down the circuits into element, serial, and parallel blocks. Please refer to section 1.5.

⑦ Branch: In any network, branch is obtained if the right side of a vertical line is connected with two or more rows of circuits.

Example:

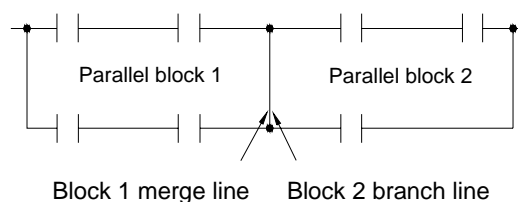


Merge line is defined as another vertical line at the right side of a branch line that merges the branch circuits into a closed circuit (forming a parallel block). This vertical line is called “Merge line”.



If both the right and the left sides of the vertical line are connected with two or more rows of circuits, then it is both a branch line and a merge line as shown in the example below.

Example:



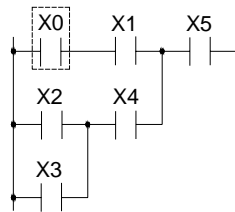
- ⑧ Network: Network is a circuit representing a specified function. It consists of the elements, branches, and blocks. Network is the basic unit in the Ladder Diagram which is capable of executing the completed functions, and the program of Ladder Diagram is formed by connecting networks together. The beginning of the network is the origin line. If two circuits are connected by a vertical line, then they belong to the same network. If there is no vertical line between the two circuits, then they belong to two different networks. Figure 1, shows three (1~3) networks.

1.4 The Coding Rules of Mnemonic (Users of WinProLadder can skip this section)

It's very easy to program FB-PLC with WinProLadder software package, just key-in the ladder symbols as they appear on your CRT screen directly to form a ladder diagram program. But for the users who are using FP-08 to program FB-PLC they have to translate ladder diagram into Mnemonic instructions by themselves. Since FP-08 only can input program with Mnemonic instruction, this section till section 1.6 will furnish you with the coding rules to translate ladder diagrams into Mnemonic instructions.

- The program editing directions are from left to right and from top to bottom. Therefore the beginning point of the network must be at the upper left corner of the network. Except the function instruction without the input control, the first instruction of a network must begin with the ORG and only one ORG instruction is permissible per network. Please refer to section 5.1.1 for further explanations.

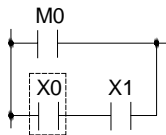
Example:



ORG	X	0
AND	X	1
LD	X	2
OR	X	3
AND	X	4
ORLD		
AND	X	5

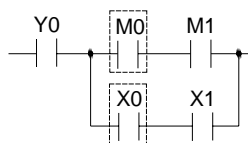
- Using LD instruction for connecting vertical lines (origin line or branch line) except at the beginning of the network.

Example 1:



ORG	M	0
LD	X	0
AND	X	1
ORLD		

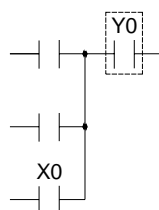
Example 2:



AND	Y	0
LD	M	0
AND	M	1
LD	X	0
AND	X	1
ORLD		

Remark 1: Using the AND instruction directly if only one row of elements is serially connected to the branch line.

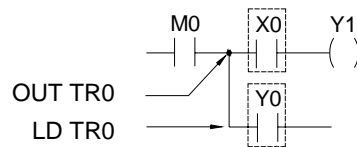
Example:



AND	X	0
ORLD		
AND	Y	0

Remark 2: Also using the AND instruction directly if an OUT TR instruction has been used at a branch line to store the node statuses.

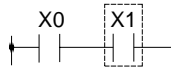
Example:



AND	M	0
OUT TR	0	
AND	X	0
OUT	Y	1
LD TR	0	
AND	Y	0

- Using AND instruction for serial connection of a single element.

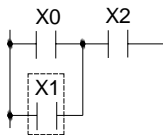
Example:



ORG	X	0
AND	X	1

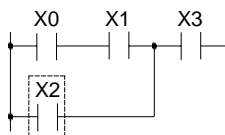
- Using OR instruction for parallel connection of a single element.

Example:



ORG	X	0
OR	X	1
AND	X	2

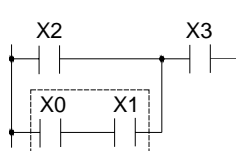
Example:



ORG	X	0
AND	X	1
OR	X	2
AND	X	3

- If the parallel element is a serial block, ORLD instruction must be used.

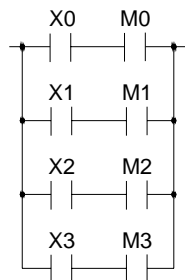
Example:



ORG	X	2
LD	X	0
AND	X	1
ORLD		
AND	X	3

Remark : If more than two blocks are to be connected in parallel, they should be connected in a top to bottom sequence. For example, block 1 and block 2 should be connected first, then connect block 3 to it and so on.

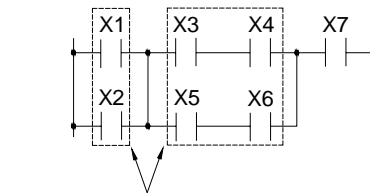
Example:



LD	X	0
AND	M	0
LD	X	1
AND	M	1
ORLD		
LD	X	2
AND	M	2
ORLD		
LD	X	3
AND	M	3

- ANDLD instruction is used to connect parallel blocks in series.

Example:



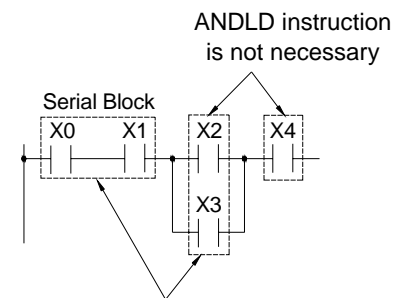
Must use ANDLD instruction



ORG	X	1
OR	X	2
LD	X	3
AND	X	4
LD	X	5
AND	X	6
ORLD		
ANDLD		
AND	X	7

- The ANDLD instruction must be used if the element or serial block is in front of the parallel block. If the parallel block is in front of the element or serial block, AND instruction can be used to connect all parts together.

Example:



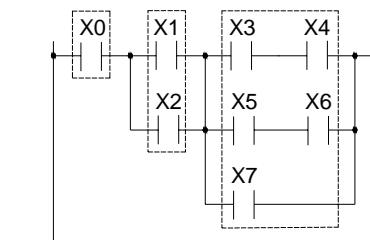
Must use ANDLD instruction



ORG	X	0
AND	X	1
LD	X	2
OR	X	3
ANDLD		
AND	X	4

Remark: If there are more than two blocks are to be connected serially, they should be connected in a top to bottom sequence. For example, block 1 and 2 should be connected first, then connect block 3 to it and so on.

Example:



ORG	X	0
LD	X	1
OR	X	2
ANDLD		
LD	X	3
AND	X	4
LD	X	5
AND	X	6
ORLD		
OR	X	7
ANDLD		

- The output coil instruction (OUT) can only be located at end of the network (the right end) and no other elements can be connected to it afterwards. The output coil can not connect to the origin line directly. If you want to connect the output coil to the origin line, connect it serially with a short circuit contact.

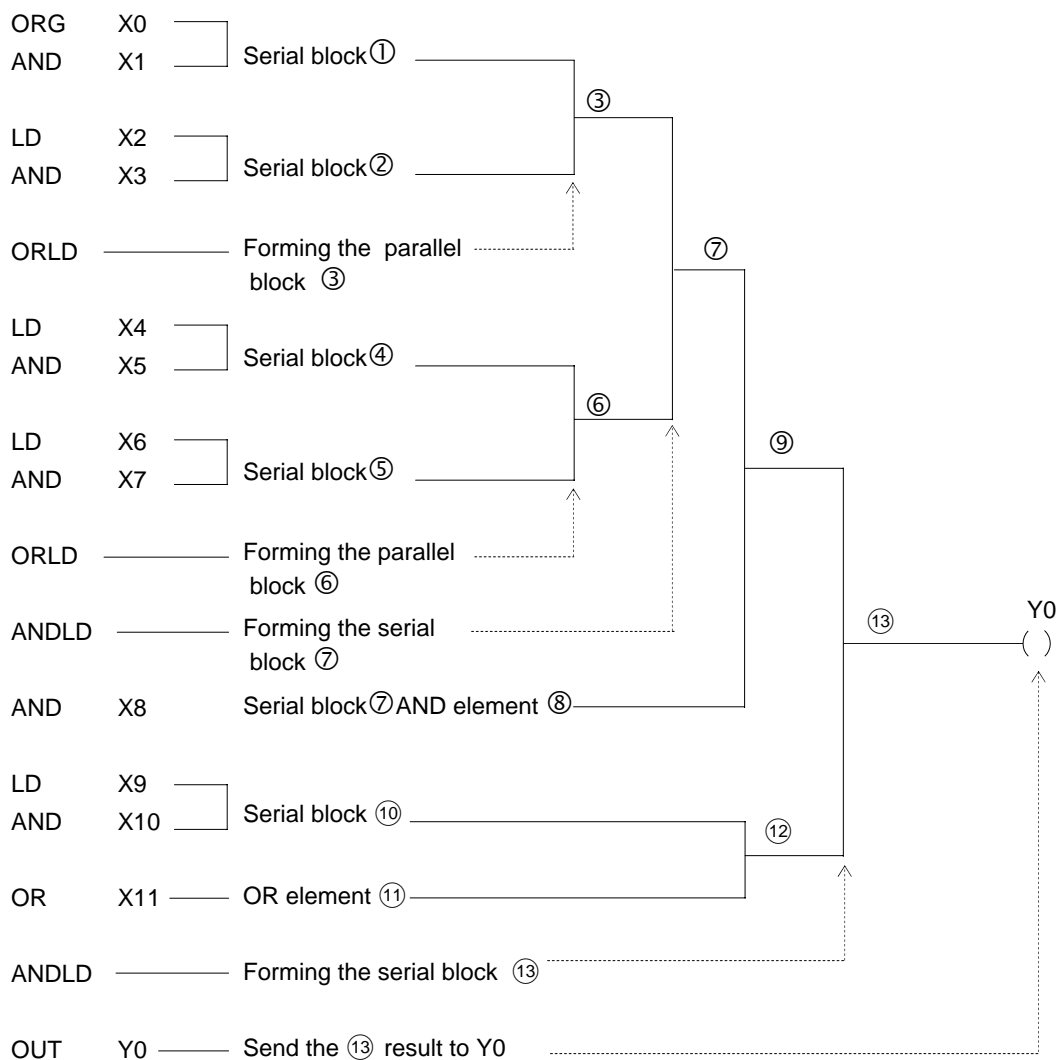
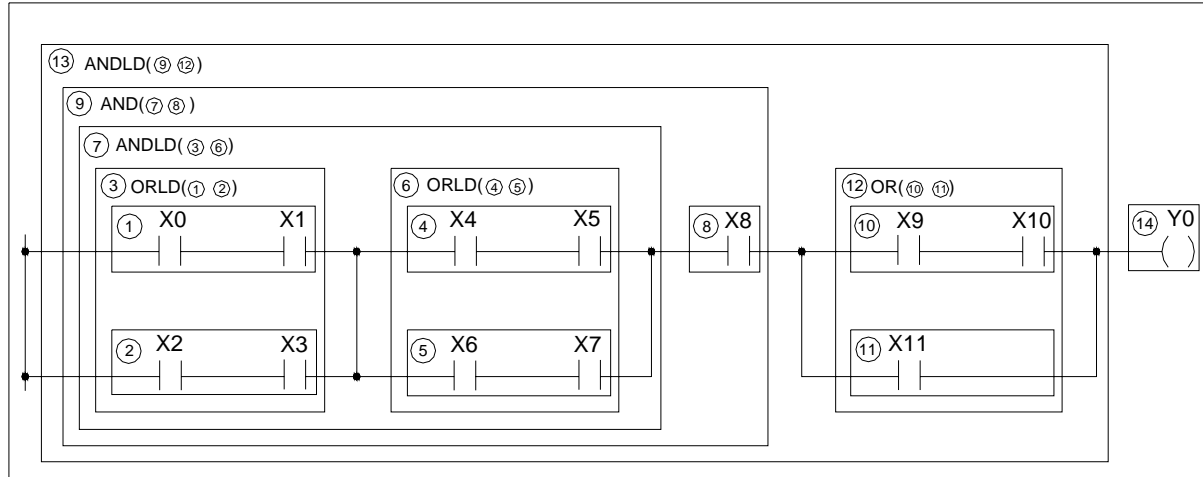


ORG SHORT
OUT Y 0

1.5 The De-Composition of a Network (Users of WinProladder can skip this section)

The key process of de-composition of a network is to separate the circuits that appear between two vertical lines into independent elements and serial blocks, then coding those elements and serial blocks according to the mnemonic coding rules and then connect them (with ANDLD or ORLD instruction) from left to right and top to bottom to form a parallel or a serial-parallel blocks, and finally to form a complete network.

Sample diagram:



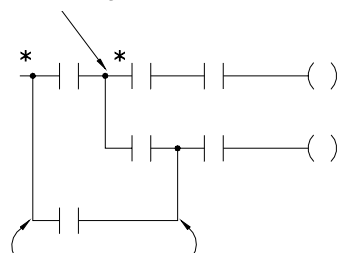
1.6 Using Temporary Relays (Users of WinProLadder can skip this section)

The network de-composition method for mnemonic coding demonstrated in section 1.5 does not apply to the branched circuit or branched block. In order to input the program using the method shown in section 1.5, It must first to store the statuses of branched nodes in temporary relays. The program design should avoid having branched circuit or branched block as much as possible. Please refer the next section "Program Simplification Techniques". Two situations that must use the TR are described at below.

- Branched circuit: Merge line does not exist at the right side of the branch line or there is a merge line at the right side of the branch line but they are not in the same row.

Example : * indicates setting of TR relay

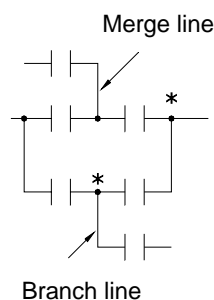
Without merge line



Although this branch has merge lines
but they are not in the same row, so this
is also a branched circuit

- Branched block : The horizontal parallel blocks with a branch in one of the blocks.

Example :



Branch line

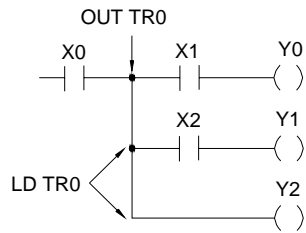
Remark 1: The OUT TR instruction must be programmed at the top of the branched point. LD TRn instruction is used at the starting point of the circuits after second rows of the branch line for regaining the branch line status before you can connect any element to the circuits. AND instruction must be used to connect the first element after OUT TRn or LD TRn instruction. LD instruction is not allowed in this case.

Remark 2: A network can have up to 40 TR points and the TR number can not be used repeatedly in the same network. It is recommended to use the numbers 1,2,3... with sequence. The TR number must be the same in the same branch line. For example, if a branch line uses OUT TR0, then starting from row 2, LD TR0 must be used for connection.

Remark 3: If the branch line of a branched circuit or a branched block is the origin line, then ORG or LD instructions can be used directly and TR contact is not necessary.

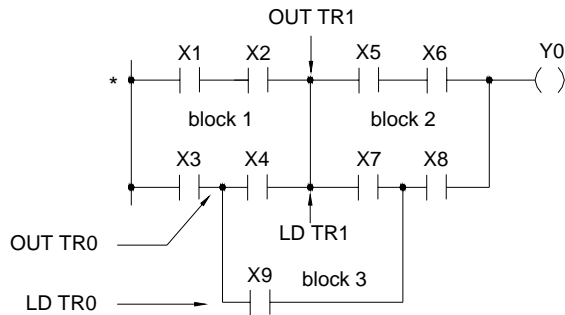
Remark 4: If any one of the branched circuit rows is not connected to the output coil (there are serially connected elements in between), and other circuits also exist after the second row, a TR instruction must be used at the branch points.

Example:



AND	X	0	
OUT TR	0		
AND	X	1	
OUT	Y	0	
LD TR	0		← Begins from row 2
AND	X	2	
OUT	Y	1	
LD TR	0		← Begins from row 3
OUT	Y	2	

Example:

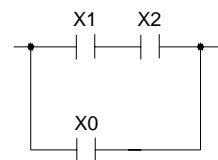
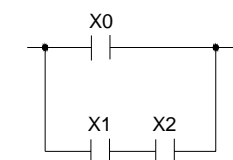


ORG	X	1	
AND	X	2	
LD	X	3	
OUT TR	0		
AND	X	4	
ORLD			
OUT TR	1		
AND	X	5	← Uses AND Instruction after TR instruction
AND	X	6	
LD TR	1		← Uses LD TR instruction to return to TR branch line
AND	X	7	
LD TR	0		
AND	X	9	← Uses AND instruction after TR instruction
ORLD			
AND	X	8	
ORLD			
OUT	Y	0	

- The above sample diagram shows a typical example of connecting two parallel blocks in series. Block 3 is formed when the element X9 is introduced into the network and the two parallel blocks become the branched blocks.
- TR instruction is not necessary because the (*) point is the origin line.
- If have already used TR relay to connect two blocks serially, then ANDLD instruction is not necessary.

1.7 Program Simplification Techniques

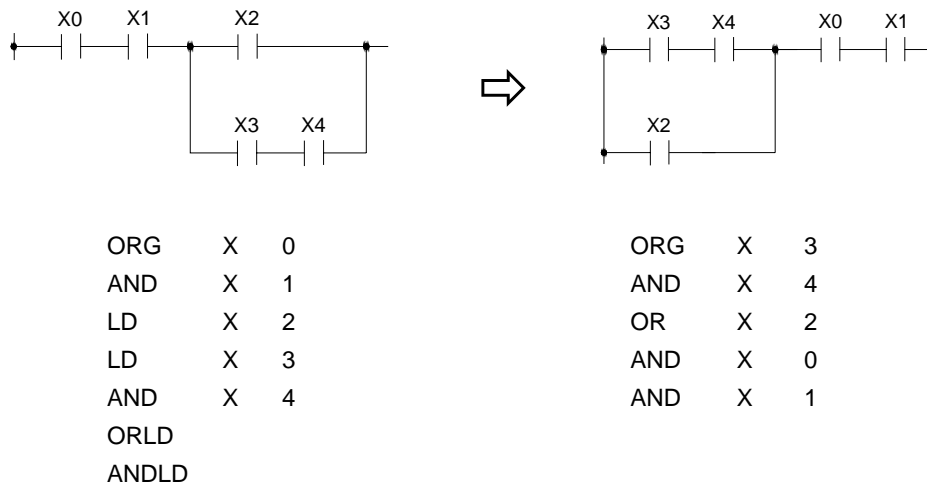
- If a single element is connected in parallel to a serial block, The ORLD instruction can be omitted if the serial block is connected on top of this single element.



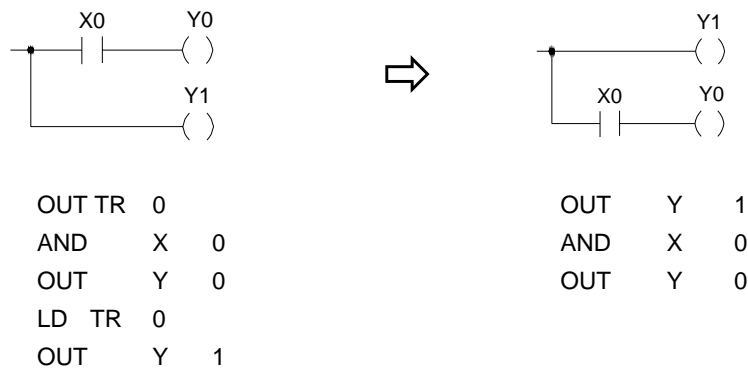
LD	X	0
LD	X	1
AND	X	2
ORLD		

LD	X	1
AND	X	2
OR	X	0

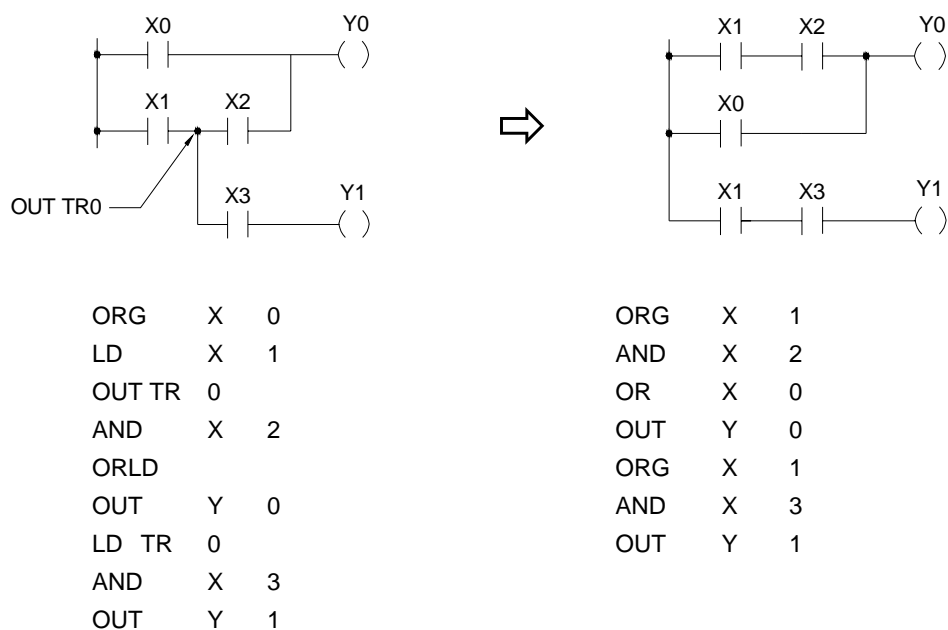
- When a single element or a serial block is connected in serial with a parallel block, ANDLD instruction can be omitted if put the parallel block in front.



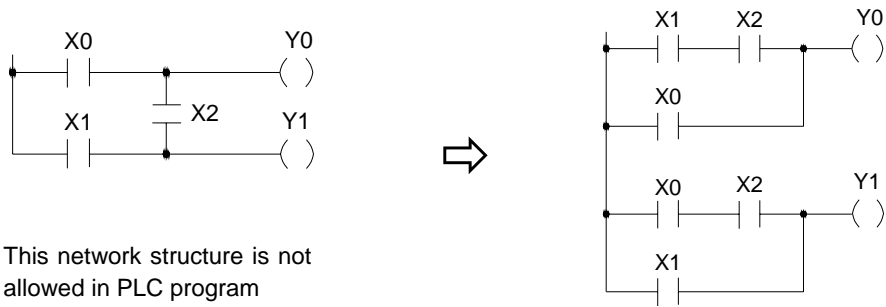
- If the branch node of a branch circuit is directly connected to the output coil, this coil could be located on top of the branch line (first row) to reduce the code.



- The diagram shown below indicates the TR relay and the ORLD instruction can be omitted.



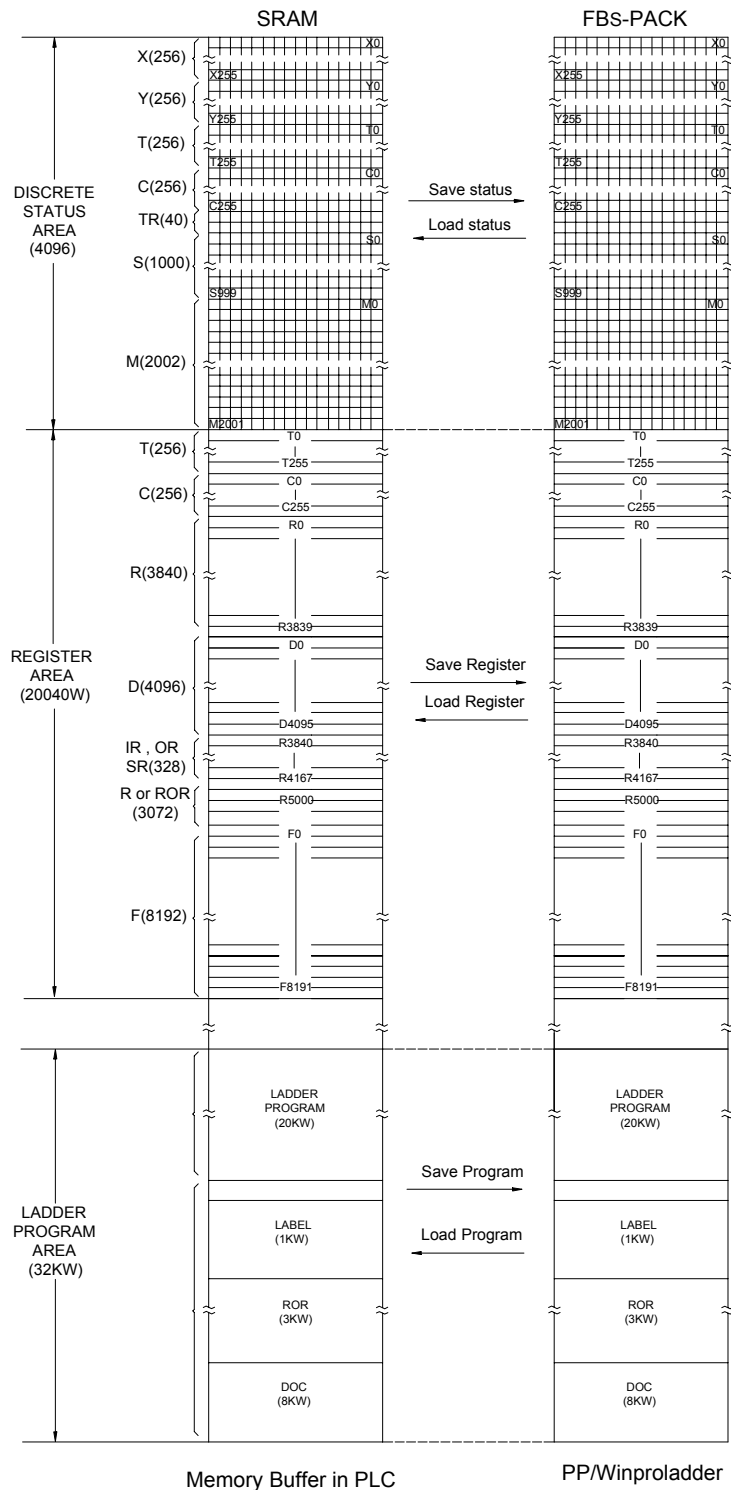
● Conversion of the bridge circuit



```
ORG X 1
AND X 2
OR X 0
OUT Y 0
ORG X 0
AND X 2
OR X 1
OUT Y 1
```

Chapter 2 FBS-PLC Memory Allocation

2.1 FBS-PLC Memory Allocation



Remark:

1. When the Read Only Register (ROR) has been configured by the user, the contents of R5000~R8071 (depends on the quantity of configuration) will be loaded from the ROR's during each time of power up or changing from STOP to RUN mode.

The user can access the ROR through the corresponding R5000~R8071.

Write operation of function instructions are prohibited in this ROR area of corresponding R5000~R8071. The others of R5000~R8071 that have not been configured for ROR, they can work as general purpose registers.

2. There is a dedicated area of program memory to store the contents of Read Only Register. ROR can be configured up to 3072 words in maximum.

2.2 Digital and Register Allocations

“*” is default, user configurable

Item				Range	Remarks
Digital 《 Bit Status 》	X	Input contact (DI)		X0 ~ X255 (256)	Corresponding to external digital input
	Y	Output relay (DO)		Y0 ~ Y255 (256)	Corresponding to external digital output
	TR	Temporary relay		TR0 ~ TR39 (40)	
	M	Internal relay	Non-retentive	M0 ~ M799 (800)*	Can be configured as retentive type
			Retentive	M1400 ~ M1911 (512)	
		Special Relay		M800 ~ M1399 (600)*	Can be configured as non-retentive type
	S	Step Relay	Non-Retentive	M1912 ~ M2001 (90)	
			Retentive	S0 ~ S499 (500)*	S20 ~ S499 can be configured as retentive type
	T	Timer “Time-Up” status contact		S500 ~ S999 (500)*	Can be configured as non-retentive type
Register 《 Word Data 》	C	Counter “Counter-Up” status contact		T0 ~ T255 (256)	
	TMR	Time current value register	0.01S Time Base	C0 ~ C255 (256)	
			0.1S Time Base	T0 ~ T49 (50)*	T0~T255 numbers for each time base can be adjusted.
			1S Time Base	T50 ~ T199 (150)*	
	CTR	Counter current value register	16-bit Retentive	T200 ~ T255 (56)*	
			16-bit Non-Retentive	C0 ~ C139 (140)*	Can be configured as non-retentive type
			32-bit Retentive	C140 ~ C199 (60)*	Can be configured as retentive type
			32-bit Non-Retentive	C200 ~ C239 (40)*	Can be configured as non-retentive type
	HR DR		Retentive	C240 ~ C255 (16)*	Can be configured as retentive type
			Non-Retentive	R0 ~ R2999 (3000)*	Can be configured as non-retentive type
			Non-Retentive	D0 ~ D3999 (4000)	
	HR ROR	Data Register	Retentive	R3000 ~ R3839 (840)*	Can be configured as retentive type
			Read Only Register (ROR)	R5000 ~ R8071 (3072) *	When not configured as ROR, it can serve normal register (for read/write)
			File Register	R5000 ~ R8071 can be set as ROR ~ default setting is (0)*	ROR is stored in special ROR area and not occupy program space
	IR	Input Register		F0 ~ F8191 (8192)	Save/retrieved via dedicated instruction
	OR	Output Register		R3840 ~ R3903 (64)	Corresponding to external numeric input
	SR	Special system register		R3904 ~ R3967 (64)	Corresponding to external numeric output
		0.1 mS High-Speed Timer Register		R3968 ~ R4167 (197) D4000 ~ D4095 (96)	
		HSC Registers	Hardware (4sets)	R4152 ~ R4154 (3)	
			Software(4sets)	DR4096 ~ DR4110 (4x4)	
		Calendar Registers	Minute	DR4112 ~ DR4126 (4x4)	
			Second	R4129	R4128
			Day	R4131	R4130
			Year	R4133	R4132
			Week		R4134

	FR	File Registers	F0~F8191(8192)	
	XR	Index Registers	V,Z (2) 、 P0~P9 (10)	

Remark: During power up or changing operation mode from STOP→RUN, all contents in non-retentive relays or registers will be cleared to 0; the retentive relays or registers will remain the same state as before.

2.3 Special Relay Details

Relay No.	Function	Description
1. Stop, Prohibited Control		
M1912	Emergency Stop control	<ul style="list-style-type: none">• If 1, PLC will be stopped (but not enter STOP mode) and all outputs OFF. This bit will be cleared when power up or changing operation mode from STOP→RUN.• All external outputs are turn off but the status of Y0～Y255 inside the PLC will not be affected.• If M2001 is 0 or enabled, the Disable/Enable status of all contacts will be reset to enable during power up or changing operation mode from STOP→RUN.• If M2001 is disabled and force ON, the Disable/Enable status & ON/OFF state of all contacts will remain as before during power up or changing operation mode from STOP→RUN. While testing, it may disable and force ON M2001 to keep the ON/OFF state of disabled contacts, but don't forget to enable the M2001 after testing.
M1913	Disable external outputs control	
M2001	Disable/Enable status retentive control	
2. CLEAR Control		
M1914	Clear Non-Retentive Relays	<ul style="list-style-type: none">• Cleared When at 1• Cleared When at 1• Cleared When at 1• Cleared When at 1• If 0, the pulse activated functions within the master control loop will only be executed once at first 0→1 of master control loop. If 1, the pulse activated functions within the master control loop will be executed every time while changing 0→1 of master control loop.
M1915	Clear Retentive Relays	
M1916	Clear Non-Retentive Registers	
M1917	Clear Retentive Registers	
M1918	Master Control (MC) Selection	
M1919	Function output control	<ul style="list-style-type: none">• If 0, the functional outputs of some function instructions will memory the output state, even these instructions not been executed. If 1, the functional output of some function instructions without the memory ability.
※ M1918/M1919 can be set to 0 or 1 at will around the whole program to meet the control requirements.		

Relay No.	Function	Description
3. Pulse Signals		
M1920 M1921 M1922 M1923 M1924 M1925 M1926	0.01S Clock pulse 0.1S Clock pulse 1S Clock pulse 60S Clock pulse } ① Initial pulse (first scan) ② Scan clock pulses ③ =0, PLC is working at STOP mode =1, PLC is working at RUN mode	<p>① "1" "0" T T T</p> <p>② M1924 t</p> <p>③ M1925 t t t t t</p> <p>t is the scan time</p> <p>T(M1920)=0.01S T(M1921)=0.1S T(M1922)=1S T(M1923)=60S</p>
M1927	CTS input status of communication port 1	<ul style="list-style-type: none"> • 0 : CTS True (ON) • 1 : CTS False (OFF) • When communication port 1 is used to connect with the printer or modem, it can use this signal and a timer to detect whether the printer or the modem is ready.
4. Error Messages		
M1928 M1929 M1930 M1931 M1932 M1933 M1934 M1935	Reserved Reserved No expansion unit or exceed the limit on number of I/O points Immediate I/O not in the main unit range Unused System stack error Reserved	<ul style="list-style-type: none"> • 1: Indicating no expansion unit or exceed the limit on number of I/O points • 1: Indicating that Immediate I/O not in the main unit range and the main unit cannot RUN • 1: Indicating that system stack error
5.Port3~Port4 Controls (MC/MN)		
M1936	Port 3 busy indicator	<ul style="list-style-type: none"> • 0 : Port 3 Busy • 1 : Port 3 Ready
M1937	Port 3 finished indicator	<ul style="list-style-type: none"> • 1 : Port 3 finished all communication transactions
M1938	Port 4 busy indicator	<ul style="list-style-type: none"> • 0 : Port 4 Busy • 1 : Port 4 Ready
M1939	Port 4 finished indicator	<ul style="list-style-type: none"> • 1 : Port 4 finished all communication transactions

Relay No.	Function	Description
6. HSC0~HSC1 Controls (MC/MN)		
M1940	HSC0 software Mask	• 1: Mask
M1941	HSC0 software Clear	• 1: Clear
M1942	HSC0 software Direction	• 0: Count-up, 1: Count-down
M1943	Reserved	
M1944	Reserved	
M1945	Reserved	
M1946	HSC1 software Mask	• 1: Mask
M1947	HSC1software Clear	• 1: Clear
M1948	HSC1 software Direction	• 0: Count-up, 1: Count-down
M1949	Reserved	
M1950	Port 3 communication indicator	• 1: Port 3 has received and transmitted a message
M1951	Port 4 communication indicator	• 1: Port 4 has received and transmitted a message
7. RTC Controls		
M1952	RTC setting	
M1953	±30 second Adjustment	
■M1954	RTC installation checking	
■M1955	Set value error	
8. Communication/Timing/Counting Controls		
M1956	Selection of Message Frame Interval Detection Time	• 0 : Use system default value as Message Frame Interval Detection Time for Modbus RTU communication protocol • 1 : Use the high byte value of R4148 as Message Frame Interval Detection Time for Modbus RTU protocol
M1957	The CV value control after the timer "Time Up"	• 0: The CV value will continue timing until the upper limit is met after "Time Up" • 1: The CV value will stop at the PV value after "Time Up" (User may control M1957 within the program to control the individual timer)
M1958	Communication port 2 High Speed Link mode selection	• 0: Set Port 2 to Normal Speed Link • 1: Set Port 2 to High Speed CPU Link ※M1958 is only effective at slave station
M1959	Modem dialing signal selection	• 0: Dialing by TONE when Port 1 connecting with Modem. • 1: Dialing by PULSE when Port 1 connecting with Modem.
M1960	Port 1 busy indicator	• 0 : Port 1 Busy • 1 : Port 1 Ready
M1961	Port 1 finished indicator	• 1 : Port 1 finished all communication transactions
M1962	Port 2 busy indicator	• 0 : Port 2 Busy • 1 : Port 2 Ready
M1963	Port 2 finished indicator	• 1 : Port 2 finished all communication transactions
M1964	Modem dialing control	• If Port 1 is connected with Modem, when signal 0→1 will dial the phone number; when signal 1→0 will hang-up the phone.

Relay No.	Function	Description
M1965	Dialing success flag	• 1: Indicating that dialing is successful (when Port 1 is connected with Modem).
M1966	Dialing fail flag	• 1: Indicating that dialing has failed (when Port 1 is connected with Modem).
M1967	Port 2 High Speed Link working mode selection	• 0: Continuous cycle. • 1: One cycle only. It will stop when the last communication transaction is completed (only effective at the master station).
M1968	Step program status	• 1: Indicating that there are more than 16 active steps in the step program at the same time.
M1969	Indirect addressing illegal write flag	• 1: Indicating that a function with index addressing attempts to write cross over the boundary of different type of data.
M1970	Port 0 status	• 1: Port 0 has received and transmitted a message
M1971	Port 1 status	• 1: Port1 has received and transmitted a message
M1972	Port 2 status	• 1: Port2 has received and transmitted a message
M1973	The CV value control after counting "Count-Up"	• 0: Indicating that the CV value will continue counting up to the upper limit after "Time-Up". • 1: Indicating that the CV value will stop at the PV value after "Count-Up" (User may control M1973 within the program to control the individual counter)
M1974	RAMP function slope control	• 0: Time control for ramping • 1: Equivalent slope control for ramping
M1975	CAM function (FUN112) selection	• 1: For the circular applications where the electric CAM switch (FUN112) can support the wrap around situation like the angle from 359° cross to 0°
9. HSC2~HSC7 Controls		
M1976	HSC2 software Mask	• 1: Mask
M1977	HSC2 software Clear	• 1: Clear
M1978	HSC2 software Direction	• 0: Count-up, 1: Count-down
M1979	HSC3 software Mask	• 1: Mask
M1980	HSC3 software Clear	• 1: Clear
M1981	HSC3 software Direction	• 0: Count-up, 1: Count-down
M1982	HSC4 software Mask	• 1: Mask
M1983	HSC4 software Direction	• 0: Count-up, 1: Count-down
M1984	HSC5 software MASK	• 1: Mask
M1985	HSC5 software Direction	• 0: Count-up, 1: Count-down
M1986	HSC6 software Mask	• 1: Mask
M1987	HSC6 software Direction	• 0: Count-up, 1: Count-down
M1988	HSC7 software Mask	• 1: Mask
M1989	HSC7 software Direction	• 0: Count-up, 1: Count-down
M1990	Reserved	

Relay No.	Function	Description
10. PSO0~POS3 Controls		
M1991	Selection of stopping the pulse output (FUN140)	• 0 : Immediately stop while stopping pulse output • 1 : Slow down stop while stopping pulse output
M1992	PSO0 Busy indicator	• 0 : PSO0 Busy • 1 : PSO0 Ready
M1993	PSO1 Busy indicator	• 0 : PSO1 Busy • 1 : PSO1 Ready
M1994	PSO2 Busy indicator	• 0 : PSO2 Busy • 1 : PSO2 Ready
M1995	PSO3 Busy indicator	• 0 : PSO3 Busy • 1 : PSO3 Ready
M1996	PSO0 Finished indicator	• 1 : PSO0 finished the last step of motion
M1997	PSO1 Finished indicator	• 1 : PSO1 finished the last step of motion
M1998	PSO2 Finished indicator	• 1 : PSO2 finished the last step of motion
M1999	PSO3 Finished indicator	• 1 : PSO3 finished the last step of motion
M2000	Selection of Multi-Axis synchronization for High Speed Pulse Output (FUN140)	• 1: Synchronized Multi-Axis

2.4 Special Registers Details

Register No.	Function	Description
R3840 R3903	Input Registers CH0 : R3840 CH63 : R3903	For Analog or Numeric inputs
R3904 R3967	Output Registers CH0 : R3904 CH63 : R3967	For Analog or Numeric outputs
R3968 R3980	Define stimulate Modbus equipment	
R3981 R3999	Reserved	
R4000	Reserved	
R4001	Reserved	
R4002	Reserved	
R4003 R4004	Define FUN86 temperature reading value at starting/end address	

Register No.	Function	Description
R4005	High Byte : Period of PWM =0, 2 seconds =1, 4 seconds =2, 8 seconds =3, 1 second =4, 16 seconds ≥5, 32 seconds Low Byte : Period of PID calculation =0, 2 seconds =1, 4 seconds =2, 8 seconds =3, 1 second =4, 16 seconds ≥5, 32 seconds	For PID temperature control
R4006	Threshold value of output ratio for heating/cooling loop abnormal detecting (Unit in %)	For PID temperature control
R4007	Threshold value of continuous time for heating/cooling loop abnormal detecting (Unit in second)	For PID temperature control
R4008	Maximum temperature for heating loop abnormal detecting	For PID temperature control
R4009	Temperature display in Celsius/Fahrenheit	=0, Celsius ;=1,Fahrenheit
R4010 R4011	Installed temperature sensor flag	Each bit represents 1 sensor, if bit value = 1 means installed.
R4012 R4013	PID Temperature control flag	Each bit represents 1 temperature point, if bit value = 1 means enable control.
R4014	Reserved	
R4015	Averaging of temperature value =0, no average on temperature =1, average by two readings =2, average by four readings =3, average by eight readings	
R4016	Reserved	
R4017	Reserved	
R4018	Reserved	
R4019	Number of PASSWORD Retry	
R4020	Control FUN148 instruction forbid to clockwise/anti-clockwise.	
R4021 R4024	Reserved	
R4025	Total Expansion Input Registers	

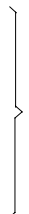
Register No.	Function	Description
R4026	Total Expansion Output Registers	
R4027	Total Expansion Digital Inputs	
R4028	Total Expansion Digital Outputs	
R4029	Reserved for system	
R4030 R4039	Tables to save or read back the data registers into or from ROM Pack	When the ROM Pack being used to save the ladder program and data registers, these tables describes which registers will be written into the ROM Pack. The addressed registers will be initialized from ROM Pack while power up.
R4040	Reply delay time settings for Port 0 and Port 1	Low Byte : For Port 0 (Unit in mS) High Byte : For Port 1 (Unit in mS)
R4041	Reply delay time settings for Port 2 and Port 3	Low Byte : For Port 2 (Unit in mS) High Byte : For Port 3 (Unit in mS)
R4042	Reply delay time settings for Port 4	Low Byte : For Port 4 (Unit in mS) High Byte : Reserved for system
R4043	Port 3 Communication Parameters Register	Set Baud Rate, Data bit...of Port 3
R4044	Port 4 Communication Parameters Register	Set Baud Rate, Data bit...of Port 4
R4045	Transmission Delay & Receive Time-out interval time Setting, while Port 3 being used as the master of FUN151 or FUN150	Low Byte : Port 3 Receive Time-out interval time (Unit in 10mS) High Byte : Port 3 Transmission Delay (Unit in 10mS)
R4046	Power up initialization mode selection of data registers that has been written into ROM Pack.	=5530H: Don't initialize the addressed data registers been written into ROM Pack while power up =Others : initialize the addressed data registers been written into ROM Pack while power up
R4047	Communication protocol setting for Port1~Port4	Set the FATEK or Modbus RTU/ASCII communication protocol
R4048	Transmission Delay & Receive Time-out interval time Setting, while Port 4 being used as the master of FUN151 or FUN150	Low Byte : Port 4 Receive Time-out interval time (Unit in 10mS) High Byte : Port 4 Transmission Delay (Unit in 10mS)
R4049	CPU Status Indication	=A55AH, Force CPU RUN =0, Normal Stop =1, Function(s) existed that CPU does not support =2, PLC ID not matched with Program ID =3, Ladder checksum error =4, System STACK error =5, Watch-Dog error =6, Immediate I/O over the CPU limitation =7, Syntax not OK =8, Qty of expansion I/O modules exceeds =9, Qty of expansion I/O points exceeds =10, CRC error of system FLASH ROM
R4050	Port 0 Communication Parameters Register	Set Baud Rate of Port 0
R4051	Reserved	
R4052	Indicator while writing ROM Pack	

Register No.	Function	Description								
R4053	Reserved									
R4054	Define the master station number of the High-Speed CPU Link network (FUN151 Mode 3)	If the master station number is 1,it can ignore this register. To set the master station number other than 1 should: Low Byte : Station number High Byte: 55H								
R4055	PLC station number	<ul style="list-style-type: none">• If high byte is not equal 55H, R4055 will show the station number of this PLC• If want to set PLC station number then R4055 should set to: Low Byte : Station number High Byte: 55H								
R4056	High Byte :Reserved Low Byte: High speed pulse output frequency dynamic control	Low Byte: =5AH, can dynamically change the output frequency of High Speed Pulse Output								
R4057	Power off counter	The value will be increased by 1 while power up								
R4058	Error station number while Port 2 in High Speed CPU Link	Used by FUN151 Mode 3 of Port 2								
R4059	Error code while Port 2 in High Speed CPU LINK mode	Used by FUN151 Mode 3 of Port 2 <table><tr><td></td><td>High byte</td><td>Low Byte</td><td></td></tr><tr><td>R4059</td><td>Err code</td><td>Err count</td><td>H</td></tr></table> Error code : 0AH, No response 01H, Framing Error 02H, Over-Run Error 04H, Parity Error 08H, CRC Error		High byte	Low Byte		R4059	Err code	Err count	H
	High byte	Low Byte								
R4059	Err code	Err count	H							

Register No.	Function	Description
R4060	Error code of PSO 0	<p>The error codes are:</p> <p>1: Parameter 0 error</p> <p>2: Parameter 1 error</p> <p>3: Parameter 2 error</p> <p>4: Parameter 3 error</p> <p>5: Parameter 4 error</p> <p>7: Parameter 6 error</p> <p>8: Parameter 7 error</p> <p>9: Parameter 8 error</p> <p>10: Parameter 9 error</p> <p>13 : Parameter 12 error</p> <p>15 : Parameter 14 error</p> <p>30: Speed setting reference number error</p> <p>31: Speed value error</p> <p>32: Stroke setting reference number error</p> <p>33: Stroke value error</p> <p>34: Illegal positioning program</p> <p>35: Step over</p> <p>36: Step number exceeds 255</p> <p>37: Highest frequency error</p> <p>38: Idle frequency error</p> <p>39: Movement compensation value too large</p> <p>40: Movement value exceeds range</p> <p>41: DRVC instruction not allow ABS addressing</p> <p>42 : DRVZ can't follow DRVC</p> <p>50 : Illegal operation mode of DRVZ</p> <p>51 : Illegal DOG input number</p> <p>52 : Illegal PG0 input number</p> <p>53 : Illegal CLR output number</p> <p>60: Illegal linear interpolation command</p>
R4061	Error code of PSO 1	Same as above
R4062	Error code of PSO 2	Same as above
R4063	Error code of PSO 3	Same as above
R4064	Being completed step number of positioning program	PSO 0
R4065		PSO 1
R4066		PSO 2
R4067		PSO 3
R4068	FUN147 GP0 vector speed	
R4069		
R4070	FUN147GP1 vector speed	
R4071		

Register No.	Function	Description
R4072 R4073 R4074 R4075 R4076 R4077 R4078 R4079	Pulse count remaining for output	Low Word of PSO 0 High Word of PSO 0 Low Word of PSO 1 High Word of PSO 1 Low Word of PSO 2 High Word of PSO 2 Low Word of PSO 3 High Word of PSO 3
R4080 R4081 R4082 R4083 R4084 R4085 R4086 R4087	Current output frequency	Low Word of PSO 0 High Word of PSO 0 Low Word of PSO 1 High Word of PSO 1 Low Word of PSO 2 High Word of PSO 2 Low Word of PSO 3 High Word of PSO 3
R4088 R4089 R4090 R4091 R4092 R4093 R4094 R4095	Current pulse position	Low Word of PSO 0 High Word of PSO 0 Low Word of PSO 1 High Word of PSO 1 Low Word of PSO 2 High Word of PSO 2 Low Word of PSO 3 High Word of PSO 3

Register No.	Function	Description
R4096	HSC0 current value Low Word	
R4097	HSC0 current value High Word	
R4098	HSC0 preset value Low Word	
R4099	HSC0 preset value High Word	
R4100	HSC1 current value Low Word	
R4101	HSC1 current value High Word	
R4102	HSC1 preset value Low Word	
R4103	HSC1 preset value High Word	
R4104	HSC2 current value Low Word	
R4105	HSC2 current value High Word	
R4106	HSC2 preset value Low Word	
R4107	HSC2 preset value High Word	
R4108	HSC3 current value Low Word	
R4109	HSC3 current value High Word	
R4110	HSC3 preset value Low Word	
R4111	HSC3 preset value High Word	
R4112	HSC4 current value Low Word	
R4113	HSC4 current value High Word	
R4114	HSC4 preset value Low Word	
R4115	HSC4 preset value High Word	
R4116	HSC5 current value Low Word	
R4117	HSC5 current value High Word	
R4118	HSC5 preset value Low Word	
R4119	HSC5 preset value High Word	
R4120	HSC6 current value Low Word	
R4121	HSC6 current value High Word	
R4122	HSC6 preset value Low Word	
R4123	HSC6 preset value High Word	
R4124	HSC7 current value Low Word	
R4125	HSC7 current value High Word	
R4126	HSC7 preset value Low Word	
R4127	HSC7 preset value High Word	
R4128	Second of calendar	
R4129	Minute of calendar	
R4130	Hour of calendar	
R4131	Day of calendar	
R4132	Month of calendar	
R4133	Year of calendar	
R4134	Day of week of calendar	
R4135	month \div minute	
<div> <div></div> <div>R4136</div> </div> <div> <div></div> <div>R4137</div> </div> <div> <div></div> <div>R4138</div> </div>	Current scan time Maximum scan time Minimum scan time	<ul style="list-style-type: none"> • Error < $\pm 1\text{ms}$ • Re-calculate when PLC changes from STOP to RUN

Register No.	Function	Description
R4139	CPU Status	Bit0 =0, PLC STOP =1, PLC RUN Bit1 , Reserved Bit2 =1, Ladder program checksum error Bit3 =0, Without ROM Pack =1, With ROM Pack Bit4 =1, Watch-Dog error Bit5 =1, MA model main unit Bit6 =1, With ID protection Bit7 =1, Emergency stop Bit8 =1, Immediate I/O over range Bit9 =1, System STACK error Bit10 =1, ASIC failed Bit11 =1, Function not allowed Bit12 , Reserved Bit13 =1, With communication board Bit14 =1, With calendar Bit15 =1, MC main unit
R4140 R4141 R4142 R4143 R4144 R4145	 Telephone Number registers	

Register No.	Function	Description
R4146	Port 1 Communication Parameters Register	Set Baud Rate, Data bit... of Port 1
R4147	Transmission Delay & Receive Time-out interval time Setting, while Port 1 being used as the master of FUN151 or FUN150	Low Byte : Port 1 Receive Time-out interval time (Unit in 10mS) High Byte : Port 1 Transmission Delay (Unit in 10mS)

Register No.	Function	Description
R4148	Message Frame Detection Time Interval	<p>.While the communication port being used as the master or slave of Modbus RTU protocol, the system will give the default time interval to identify each packet of receiving message; except this, the user can set this time interval through the high byte setting of R4148 and let M1956 be 1, to avoid the overlap of different packet of message frame.</p> <p>M1956=1, High Byte of R4148 is used to set the new message detection time interval for Port 1~Port 4 (Unit in mS)</p> <p>.While the communication port being used to communicate with the intelligent peripherals through FUN151 instruction, if the communication protocol without the end of text to separate each packet of message frame, it needs message detection time interval to identify the different packet. High byte of R4148 is used for this setting for Port 1~Port 4. (Unit in mS)</p>
R4149	Modem Interface Setting & Port0 without checking of station number for FATEK's external communication protocol	<ul style="list-style-type: none"> • High Byte of R4149: =55H, Remote-Diagnosis/Remote-CPU-Link by way of Port 1 through Modem connection, it supports user program controlled dial up function =AAH, Remote diagnosis by way of Port 1 through Modem connection, it supports Passive receiving & Active dialing operation mode =Others, without above function • Low Byte of R4149: =1, Port 0 without checking of station number for FATEK's external communication protocol (communicating with MMI/SCADA) =Others, Port 0 checks station number, it allows multi-drop network for data acquisition.
R4150	Power on I/O service delay time setting	<ul style="list-style-type: none"> • PLC is ready for I/O service after this delay time while power up. The unit is in 0.01S. The default value is 100.
R4151	Circular 1mS time base timer	<ul style="list-style-type: none"> • The content of R4151 will be increased by 1 every 1mS. It can be used for a more precise timing application.
R4152	Low word of HSTA CV register	HSTA is high speed timer in 0.1 mS resolution
R4153	High word of HSTA CV register	The HSTA can act as 32-bit cyclic timer or fixed time interrupt timer
R4154	PV register of HSTA	


Register No.	Function	Description																
R4155	Port 1 & Port 2 without station number checking for FATEK's external communication protocol	<ul style="list-style-type: none">• Low Byte of R4155: =1, Port 1 without station number checking for FATEK's external communication protocol (communicating with MMI/SCADA) ≠1,Port 1 checks station number, it allows multi-drop network for data acquisition• High Byte of R4155: =1, Port 2 without station number checking for FATEK's external communication protocol (communicating with MMI/SCADA) ≠1,Port 2 checks station number, it allows multi-drop network for data acquisition																
R4156	Port 3 & Port 4 without station number checking for FATEK's external communication protocol	<ul style="list-style-type: none">• Low Byte of R4156: =1, Port 3 without station number checking for FATEK's external communication protocol (communicating with MMI/SCADA) ≠1,Port 3 checks station number, it allows multi-drop network for data acquisition• High Byte of R4156: =1, Port 4 without station number checking for FATEK's external communication protocol (communicating with MMI/SCADA) ≠1,Port 4 checks station number, it allows multi-drop network for data acquisition																
R4157	PLC OS Version																	
R4158	Port 2 Communication Parameters Register (Not for High Speed CPU Link)	Set Baud Rate, Data bit...of Port 2																
R4159	Transmission Delay & Receive Time-out interval time Setting, while Port 2 being used as the master of FUN151 or FUN150	Low Byte : Port 2 Receive Time-out interval time (Unit in 10mS) High Byte : Port 2 Transmission Delay (Unit in 10mS)																
R4160	Port2 RX/TX time out setting for High Speed CPU Link	High Byte of R4160 : =56H, User setting mode if the system default works not well, Low Byte of R4160 is used for this setting (Not suggest) =Others, system will give the default value according to the setting of R4161																
R4161	Port 2 Communication Parameters Register (For High Speed CPU Link)	<ul style="list-style-type: none">•Set Baud Rate, Parity...of Port 2• Data bit is fixed to 8-bit• Baud Rate≥38400 bps																
R4162	Fixed time interrupt enable/disable control	<table><tr><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr><tr><td>100mS</td><td>50mS</td><td>10mS</td><td>5mS</td><td>4mS</td><td>3mS</td><td>2mS</td><td>1mS</td></tr></table> Bit=0, interrupt enabled Bit=1, interrupt disabled	B7	B6	B5	B4	B3	B2	B1	B0	100mS	50mS	10mS	5mS	4mS	3mS	2mS	1mS
B7	B6	B5	B4	B3	B2	B1	B0											
100mS	50mS	10mS	5mS	4mS	3mS	2mS	1mS											

Register No.	Function	Description
R4163	Modem dialing control setting	<ul style="list-style-type: none"> • Low Byte of R4163 : <ul style="list-style-type: none"> =1, Ignore the dialing tone and the busy tone when dialing. =2, Wait the dialing tone but ignore the busy tone when dialing. =3, Ignore the dialing tone but detect the busy tone when dialing. =4, Wait the dialing tone and detect the busy tone when dialing. =Any other value treated as value equal 4. • High Byte of R4163 : The Ring count setting for Modem auto answer
R4164	V index register	
R4165	Z index register	
R4166	System used	
R4167	Model of main unit	<ul style="list-style-type: none"> • Low Byte of R4167: <ul style="list-style-type: none"> =0, 6I + 4O (FBs-10xx) =1, 8I + 6O (FBs-14xx) =2, 12I + 8O (FBs-20xx) =3, 14I + 10O (FBs-24xx) =4, 20I + 12O (FBs-32xx) =5, 24I + 16O (FBs-40xx) =6, 36I + 24O (FBs-60xx) =7, 28I + 16O (FBs-44MN) • High Byte of R4167: <ul style="list-style-type: none"> =0, MA =1, MC =2, MN

Register No.	Function	Description
D4000	Port 1 User-defined Baud Rate Divisor (R4146 must be 56XFH)	Port 1 user-defined Baud Rate (1125~1152000 bps) $D4000 = (18432000/\text{Baud Rate}) - 1$
D4001	Port 2 User-defined Baud Rate Divisor (R4158 must be 56XFH)	Port 2 user-defined Baud Rate (1125~1152000 bps) $D4001 = (18432000/\text{Baud Rate}) - 1$
D4002	Port 3 User-defined Baud Rate Divisor (R4043 must be 56XFH)	Port 3 user-defined Baud Rate (1125~1152000 bps) $D4002 = (18432000/\text{Baud Rate}) - 1$
D4003	Port 4 User-defined Baud Rate Divisor (R4044 must be 56XFH)	Port 4 user-defined Baud Rate (1125~1152000 bps) $D4003 = (18432000/\text{Baud Rate}) - 1$
D4004	FUN30 PID resolution of analog input	=0, 14-bit format but valid 12-bit resolution =1, 14-bit format and valid 14-bit resolution
D4005	FUN30 PID gain constant	$KC = D4005/Pb$

Register No.	Function	Description
D4006 D4042	Analog input valid bit and set times of average	
D4043 D4045	Communication function setting	
D4046 D4052	Reserved	
D4053 D4054	RTC chip RTC time setup	RTC chip is S35390A, is able through D4054 to do time setup
D4055 D4059	Reserved	
D4060 D4061 D4062 D4063	FUN147 GP0 error code FUN147 GP1 error code FUN147 the step number (positioning point) which has been completed of GP0 FUN147 the step number (positioning point) which has been completed of GP1	
D4064 D4070	Reserved	
D4071 D4079	Used in FBs-B2A1D/FBs-B2DA/ FBs-B4AD	
D4080 D4081 D4082 D4083 D4084 D4085 D4086 D4087 D4088 D4089	P0 index register P1 index register P2 index register P3 index register P4 index register P5 index register P6 index register P7 index register P8 index register P9 index register	
D4090 D4095	Reserved	

Remark: All the special relays or registers attached with “” symbol shown in the above table are write prohibited.

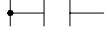

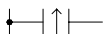

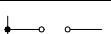
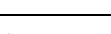
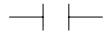
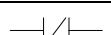
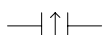

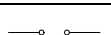
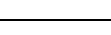
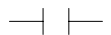
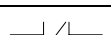
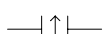
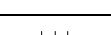
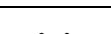
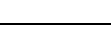

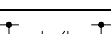
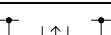
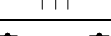
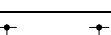
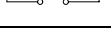
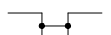
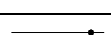
For the special relays attached with “” symbol also has following characteristics

. Forced and Enable/Disable operation is not allowed.

. Can't be referenced by TU/TD transitional contact (contact will always open)

Chapter 3 FBS-PLC Instruction Lists

3.1 Sequential Instructions

Instruction	Operand	Symbol	Function Descriptions	Execution Time	Instruction type
ORG	X,Y,M, S,T,C		Starting a network with a normally open (A) contact	0.33uS	Network starting instructions
ORG NOT			Starting a network with a normally closed (B) contact		
ORG TU			Starting a network with a differential up (TU) contact	0.54uS	
ORG TD			Starting a network with a differential down (TD) contact		
ORG OPEN			Starting a network with a open circuit contact	0.33uS	
ORG SHORT			Starting a network with a short circuit contact		
LD	X,Y,M, S,T,C		Starting a relay circuit from origin or branch line with a normally open contact	0.33uS	Origin or branch line starting instructions
LD NOT			Starting a relay circuit from origin or branch line with a normally closed contact		
LD TU			Starting a relay circuit from origin or branch line with a differential up contact	0.54uS	
LD TD			Starting a relay circuit from origin or branch line with a differential down contact		
LD OPEN			Starting a relay circuit from origin or branch line with a open circuit contact	0.33uS	
LD SHORT			Starting a relay circuit from origin or branch line with a short circuit contact		
AND	X,Y,M, S,T,C		Serial connection of normally open contact	0.33uS	Serial connection instructions
AND NOT			Serial connection of normally closed contact		
AND TU			Serial connection of differential up contact	0.54uS	
AND TD			Serial connection of differential down contact		
AND OPEN			Serial connection of open circuit contact	0.33uS	
AND SHORT			Serial connection of short circuit contact		
OR	X,Y,M, S,T,C		Parallel connection of normally open contact	0.33uS	Parallel connection instructions
OR NOT			Parallel connection of normally closed contact		
OR TU			Parallel connection of differential up contact	0.54uS	
OR TD			Parallel connection of differential down contact		
OR OPEN			Parallel connection of open circuit contact	0.33uS	
OR SHORT			Parallel connection of short circuit contact		
ANDLD			Serial connection of two circuit blocks	0.33uS	Blocks merge instructions
ORLD			Parallel connection of two circuit blocks		

Instruction	Operand	Symbol	Function Descriptions	Execution Time	Instruction type
OUT	Y,M,S	—()	Send result to coil	0.33uS 1.09uS	Coil output instruction
OUT NOT		—(/)	Send inverted result to coil		
OUT	Y	—(L)	Send result to an external output coil and appoint it as of retentive type	1.09uS	
OUT L	TR		Save the node status to a temporary relay	0.33uS	Node operation instruction
LD			Load the temporary relay		
TU		—↑—	Take the transition up of the node status	0.33uS	
TD		—↓—	Take the transition down of the node status	0.33uS	
NOT		—/—	Invert the node status	0.33uS	
SET		—(S)	Set a coil	0.33uS 1.09uS	
RST		—(R)	Reset a coil	0.33uS 1.09uS	

● The 36 sequential instructions listed above are all applicable to every models of FBs-PLC.

3.2 Function Instructions

There are more than 100 different FBs-PLC function instructions. If put the **D** and **P** derivative instructions into account, the total number of instructions is over 300. On top of these, many function instructions have multiple input controls (up to 4 inputs) which can have up to 8 different types of operation mode combinations. Hence, the size of FBs-PLC instruction sets is in fact not smaller than that of a large PLC. Having powerful instruction functions, though may help for establishing the complicated control applications, but also may impose a heavy burden on those users of small type PLC's. For ease of use, FATEK PLC function instructions are divided into two groups, the Basic function group which includes 26 commonly used function instructions and 4 SFC instructions and the advanced function group which includes other more complicated function instructions, such as high-speed counters and interrupts. This will enable the beginners and the non-experienced users to get familiar with the basic function very quickly and to assist experienced users in finding what they need in the advanced set of function instructions.

The instructions attached with “★” symbol are basic functions which amounts to 26 function instructions and 4 SFC instructions. All the basic functions will be explained in next chapter. The details for the reset of functions please refer advanced manual.

■ General Timer/Counter Function Instructions

FUN No.	Name	Operand	Derivative Instruction	Function descriptions
★	T nnn	PV		General timer instructions ("nnn" range 0~255, total 256)
★	C nnn	PV		General counter instructions ("nnn" range 0~255, total 256)
★ 7	UDCTR	CV,PV	DP	16-Bit or 32-Bit up/down counter

■ Single Operand Function Instructions

★ 4	DIFU	D	P	To get the up differentiation of a D relay and store the result to D
★ 5	DIFD	D	P	To get the down differentiation of a D relay and store the result to D
★ 10	TOGG	D	P	Toggle the status of the D relay

■ Setting/Resetting

★	SET	D	DP	Set all bits of register or a discrete point to 1
★	RST	D	DP	Clear all bits of register or a discrete point to 0
114	Z-WR	N	P	Zone set or clear

■ SFC Instructions

★	STP	Snnn		STEP declaration
★	STPEND			End of the STEP program
★	TO	Snnn		STEP divergent instruction
★	FROM	Snnn		STEP convergent instruction

■ Mathematical Operation Instructions

★ 11	(+)	Sa,Sb,D	DP	Perform addition of Sa and Sb and then store the result to D
★ 12	(-)	Sa,Sb,D	DP	Perform subtraction of Sa and Sb and then store the result to D
★ 13	(*)	Sa,Sb,D	DP	Perform multiplication of Sa and Sb and then store the result to D
★ 14	(/)	Sa,Sb,D	DP	Perform division of Sa and Sb and then store the result to D
★ 15	(+1)	D	DP	Adds 1 to the D value
★ 16	(-1)	D	DP	Subtracts 1 from the D value
23	DIV48	Sa,Sb,D	P	Perform 48 bits division of Sa and Sb and then store the result to D
24	SUM	S,N,D	DP	Take the sum of the successive N values beginning from S and store it in D
25	MEAN	S,N,D	DP	Take the mean average of the successive N values beginning from S and store it in D
26	SQRT	S,D	DP	Take the square root of the S value and store it in D
27	NEG	D	DP	Take the 2's complement (negative number) of the D value and store it back in D
28	ABS	D	DP	Take the absolute value of D and store it back in D
29	EXT	D	P	Take the 16 bit numerical value and extend it to 1 32 bit numerical value (value will not change)
30	PID	TS,SR,OR,PR,WR		PID operation
31	CRC	MD,S,N,D	P	CRC16 checksum calculation
32	ADCNV	PI,S,N,D		Offset and full scale conversion

FUN No.	Name	Operand	Derivative Instruction	Function descriptions
33	LCNV	Md,S,Ts,D,L	P	Linear Conversion
34	MLC	Rs,SI,Tx,Ty,TI, D	P	Multiple Linear Conversion
200	I→F	S,D	DP	Integer to floating point number conversion
201	F→I	S,D	DP	Floating point number to integer conversion
202	FADD	Sa,Sb,D	P	Addition of floating point number
203	FSUB	Sa,Sb,D	P	Subtraction of floating point number
204	FMUL	Sa,Sb,D	P	Multiplication of floating point number
205	FDIV	Sa,Sb,D	P	Division of floating point number
206	FCMP	Sa,Sb	P	Comparison of floating point number
207	FZCP	Sa,Sb	P	Zone comparison of floating point number
208	FSQR	S,D	P	Square root of floating point number
209	FSIN	S,D	P	SIN trigonometric function
210	FCOS	S,D	P	COS trigonometric function
211	FTAN	S,D	P	TAN trigonometric function
212	FNEG	D	P	Change sign of floating point number
213	FABS	D	P	Take absolute value of floating point number
214	FLN	S,D	P	Floating point napierian logarithm
215	FEXP	S,D	P	Floating point exponential function
216	FLOG	S,D	P	Floating point logarithm
217	FPOW	Sy, Sx,D	P	Floating point power function
218	FASIN	S,D	P	Floating point arc sine function
219	FACOS	S,D	P	Floating point arc cosine function
220	FATAN	S,D	P	Floating point arc tangent function

■ Logical Operation Instructions

★ 18	AND	Sa,Sb,D	DP	Perform logical AND for Sa and Sb and store the result to D
★ 19	OR	Sa,Sb,D	DP	Perform logical OR for Sa and Sb and store the result to D

35	XOR	Sa,Sb,D	D P	Take the result of the Exclusive NOR logical operation made between Sa and Sb, and store it in D
36	XNR	Sa,Sb,D	D P	Take the result of the Exclusive NOR logical operation made between Sa and Sb, and store it in D

■ Comparison Instructions

★ 17	CMP	Sa,Sb	D P	Compare the data at Sa and data at Sb and output the result to function outputs (FO0~FO2)
37	ZNCMP	S,Su,SL	D P	Compare S with the zones formed by the upper limit Su and lower limit SL, and set the result to FO0~FO2

■ In Line Comparison Instructions

170	=	Sa,Sb	D	Equal to compare
171	>	Sa,Sb	D	Greater than compare
172	<	Sa,Sb	D	Less than compare
173	< >	Sa,Sb	D	Not equal to compare
174	> =	Sa,Sb	D	Greater than or equal to compare
175	= <	Sa,Sb	D	Less than or equal to compare

■ Data Movement Instructions

FUN No.	Name	Operand	Derivative instruction	Function descriptions
★ 8	MOV	S,D	D P	Transfer the W or DW data specified at S to D
★ 9	MOV/	S,D	D P	Invert the W or DW data specified at S, and then transfers the result to D
40	BITRD	S,N	D P	Read the status of the bits specified by N within S, and send it to FO0
41	BITWR	D,N	D P	Write the INB input status into the bits specified by N within D
42	BITMV	S,Ns,D,Nd	D P	Write the status of bit specified by N within S into the bit specified by N within D
43	NBMV	S,Ns,D,Nd	D P	Write the Ns nibble within S to the Nd nibble within D
44	BYMV	S,Ns,D,Nd	D P	Write the byte specified by Ns within S to the byte specified by Nd within D
45	XCHG	Da,Db	D P	Exchange the values of Da and Db
46	SWAP	D	P	Swap the high-byte and low-byte of D
47	UNIT	S,N,D	P	Take the nibble 0 (NB0) of the successive N words starting from S and combine the nibbles sequentially then store in D
48	DIST	S,N,D	P	De-compose the word into successive N nibbles starting from nibble 0 of S, and store them in the NB0 of the successive N words starting from D
49	BUNIT	S,N,D	P	Low byte of words re-unit

FUN No.	Name	Operand	Derivative instruction	Function descriptions
50	BDIST	S,N,D	P	Words split into multi-byte
160	RW-FR	Sa,Sb,Pr,L	DP	File register access
161	WR-MP	S, Bk,Os, Pr,L,WR	P	Write memory pack
162	RD- MP	Bk,Os,Pr L,D PR,WR	P	Read memory pack

■ Shifting/Rotating Instructions

★ 6	BSHF	D	DP	Shift left or right 1 bit of D register
51	SHFL	D,N	DP	Shift left the D register N bits and move the last shifted out bits to OTB. The empty bits will be replaced by INB input bit
52	SHFR	D,N	DP	Shift right the D register N bits and move the last shifted out bits to OTB, The empty bits will be replaced by INB input bit
53	ROTL	D,N	DP	Rotate left the D operand N bits and move the last rotated out bits to OTB
54	ROTR	D,N	DP	Rotate right the D operand N bits and move the last rotated out bits to OTB

■ Code Conversion Instruction

★ 20	→BCD	S,D	DP	Convert binary data of S into BCD data and store the result to D
★ 21	→BIN	S,D	DP	Convert BCD data of S into binary data and store the result to D
55	B→G	S,D	DP	Binary to Gray code conversion
56	G→B	S,D	DP	Gray code to Binary conversion
57	DECOD	S,Ns,NL,D	P	Decode the binary data formed by NL bits starting from Ns bit within S, and store the result in the register starting from D
58	ENCOD	S,Ns,NL,D	P	Encoding the NL bits starting from the Ns bit within S, and store the result in D
59	→7SG	S,N,D	P	Convert the N+1 number of nibble data within S, into 7 segment code, then store in D
60	→ASC	S,D	P	Write the constant string S (max. 12 alpha-numeric or symbols) into the registers starting from D
61	→SEC	S,D	P	Convert the time data (hours, minutes, seconds) of the three successive registers starting from S into seconds data then store to D
62	→HMS	S,D	P	Convert the seconds data of S into time data (hours, minutes, seconds) and store the data in the three successive registers starting from D
63	→HEX	S,N,D	P	Convert the successive N ASCII data starting from S into hexadecimal data and store them to D

64	→ASC II	S,N,D	P	Convert the successive N hexadecimal data starting from S into ASCII codes and store them to D
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■ Flow Control Instructions

★ 0	MC	N		The start of master control loop
★ 1	MCE	N		The end of master control loop
★ 2	SKP	N		The start of skip loop
★ 3	SKPE	N		The end of skip loop
	END			End of Program
22	BREAK		P	Exit from FOR-NEXT loop
65	LBL	1~6 alphanumeric		Define the label with 1~6 alphanumeric characters
66	JMP	LBL	P	Jump to LBL label and continues the program execution
67	CALL	LBL	P	Call the sub-program begin with LBL label
68	RTS			Return to the calling main program from sub-program
69	RTI			Return to interrupted main program from sub-program
70	FOR	N		Define the starting point of the FOR Loop and the loop count N
71	NEXT			Define the end of FOR loop

■ I/O Function Instructions

FUN No.	Name	Operand	Derivative instruction	Function descriptions
74	IMDIO	D,N	P	Update the I/O signal on the main unit immediately
76	TKEY	IN,D,KL	D	Convenient instruction for 10 numeric keys input
77	HKEY	IN,OT,D,KL	D	Convenient instruction for 16 keys input
78	DSW	IN,OT,D	D	Convenient instruction for digital switch input
79	7SGDL	S,OT,N	D	Convenient instruction for multiplexing 7-segment display
80	MUXI	IN,OT,N,D		Convenient instruction for multiplexing input instruction
81	PLSO	MD, Fr, PC UY,DY,HO	D	Pulse output function (for bi-directional drive of step motor)
82	PWM	TO,TP,OT		Pulse width modulation output function
83	SPD	S,TI,D		Speed detection function
84	TDSP	S,Yn,Dn, PT,IT,WS		7/16-segment LED display control
86	TPCTL	Md,Yn,Sn,Zn, Sv,Os,PR IR,DR,OR,WR		PID Temperature control
139	HSPWM	PW,OP,RS, PN,OR,WR		High Speed PWM pulse output

■ Cumulative Timer Function Instructions

87	T.01S	CV,PV		Cumulative timer using 0.01S as the time base
88	T.1S	CV,PV		Cumulative timer using 0.1S as the time base
89	T1S	CV,PV		Cumulative timer using 1S as the time base

■ Watch Dog Timer Control Function Instructions

90	WDT	N	P	Set the WDT timer time out time to N mS
91	RSWDT		P	Reset the WDT timer to 0

■ High Speed Counter Control Function Instructions

92	HSCTR	CN	DP	Read the current CV value of the hardware HSCs, HSC0~HSC3, or HST on ASIC to the corresponding CV register in the PLC respectively
93	HSCTW	S,CN,D	DP	Write the CV or PV register of HSC0~HSC3 or HST in the PLC to CV or PV register of the hardware HSC or HST on ASIC respectively

■ Report Function Instructions

94	ASCWR	MD,S,Pt	P	Parse and generate the report message based on the ASCII formatted data starting from the address S. Then report message will send to port1
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■ Ramp Function Instructions

FUN No.	Name	Operand	Derivative instruction	Function descriptions
95	RAMP	Tn,PV,SL, SU,D	P	Ascending/Descending convenient instruction
98	RAMP2	Om,Ta Td,Rt Rc,WR		Tracking type ramp function for D/A output

■ Communication Function Instructions

150	M-Bus	Pt, SR, WR	P	Modbus protocol communication
151	CLINK	PT, WD, SR, WR	P	FATEK/Generic protocol communication

■ Table Function Instructions

100	R→T	Rs,Td,L,Pr	DP	Store the Rs value into the location pointed by the Pr in Td
101	T→R	Ts,L,Pr,Rd	DP	Store the value at the location pointed by the Pr in Ts into Rd
102	T→T	Ts,Td,L,Pr	DP	Store the value at the location pointed by the Pr in Ts into the location pointed by the Pr in Td
103	BT_M	Ts,Td,L	DP	Copy the entire contents of Ts to Td
104	T_SWP	Ta,Tb,L	DP	Swap the entire contents of Ta and Tb
105	R-T_S	Rs,Ts,L,Pr	DP	Search the table Ts to find the location with data different or equal to the value of Rs. If found store the position value into the Pr
106	T-T_C	Ta,Tb,L,Pr	DP	Compare two tables Ta and Tb to search the entry with different or same value. If found store the position value into the Pr
107	T_FIL	Rs,Td,L	DP	Fill the table Td with Rs
108	T_SHF	IW,Ts,Td, L,OW	DP	Store the result into Td after shift left or right one entry of table Ts. The shift out data is send to OW and the shift in data is from IW
109	T_ROT	Ts,Td,L	DP	Store the result into Td after shift left or right one entry of table Ts.
110	QUEUE	IW,QU,L, Pr,OW	DP	Push IW into QUEUE or get the data from the QUEUE to OW (FIFO)
111	STACK	IW,ST,L, Pr,OW	DP	Push IW into STACK or get the data from the STACK to OW (LIFO)
112	BKCMP	Rs,Ts,L,D	DP	Compare the Rs value with the upper/lower limits of L, constructed by the table Ts, then store the comparison result of each pair into the relay designated by D (DRUM)
113	SORT	S,D,L	DP	Sorting the registers starting from S length L and store the sorted result to D

■ Matrix Instructions

120	MAND	Ma,Mb,Md,L	P	Store the results of logic AND operation of Ma and Mb into Md
121	MOR	Ma,Mb,Md,L	P	Store the results of logic OR operation of Ma and Mb into Md
122	MXOR	Ma,Mb,Md,L	P	Store the results of logic Exclusive NOR operation of Ma and Mb into Md
123	MXNR	Ma,Mb,Md,L	P	Store the results of logic Exclusive NOR operation of Ma and Mb into Md
124	MINV	Ms,Md ,L	P	Store the results of inverse Ms into Md
125	MCMP	Ma,Mb,L Pr	P	Compare Ma and Mb to find the location with different value, then store the location into Pr
126	MBRD	Ms,L,Pr	P	Read the bit status pointed by the Pr in Ms to the OTB output
127	MBWR	Md,L,Pr	P	Write the INB input status to the bits pointed by the Pr in Ms
128	MBSHF	Ms,Md,L	P	Store the results to Md after shift one bit of the Ms. Shifted out bit will appear at OTB and the shift in bits comes from INB
129	MBROT	Ms,Md,L	P	Store the results to Md after rotate one bit of the Ms. Rotated out bit will appear at OTB.
130	MBCNT	Ms,L,D	P	Calculate the total number of bits that are 0 or 1 in Ms, then store the results into D

■ NC Positioning Instruction

140	HSPSO	Ps,SR,WR		HSPSO instruction of NC positioning control
141	MPARA	Ps,SR		Parameter setting instruction of NC positioning control
142	PSOFF	Ps	P	Stop the pulse output of NC positioning control
143	PSCNV	Ps,D	P	Convert the Ps positions of NC positioning to mm, Inch or Deg
147	MHSPO	Gp,SR WR,		Multi-Axis high speed pulse output
148	MPG	Sc,Ps,Fo,Mr,W		Manual pulse generator for positioning

■ Disable/Enable Control of Interrupt or Peripheral


145	EN	LBL	P	Enable HSC, HST, external INT or peripheral operation
146	DIS	LBL	P	Disable HSC, HST, external INT or peripheral operation

Chapter 4 Sequential Instructions

The sequential instructions of FBs-PLC shown in this chapter are also listed in section 3.1. Please refer to Chapter 1, "PLC Ladder diagram and the Coding rules of Mnemonic instruction", for the coding rules in applying those instructions. In this chapter, we only introduce the applicable operands, ranges and element characteristics, functionality.

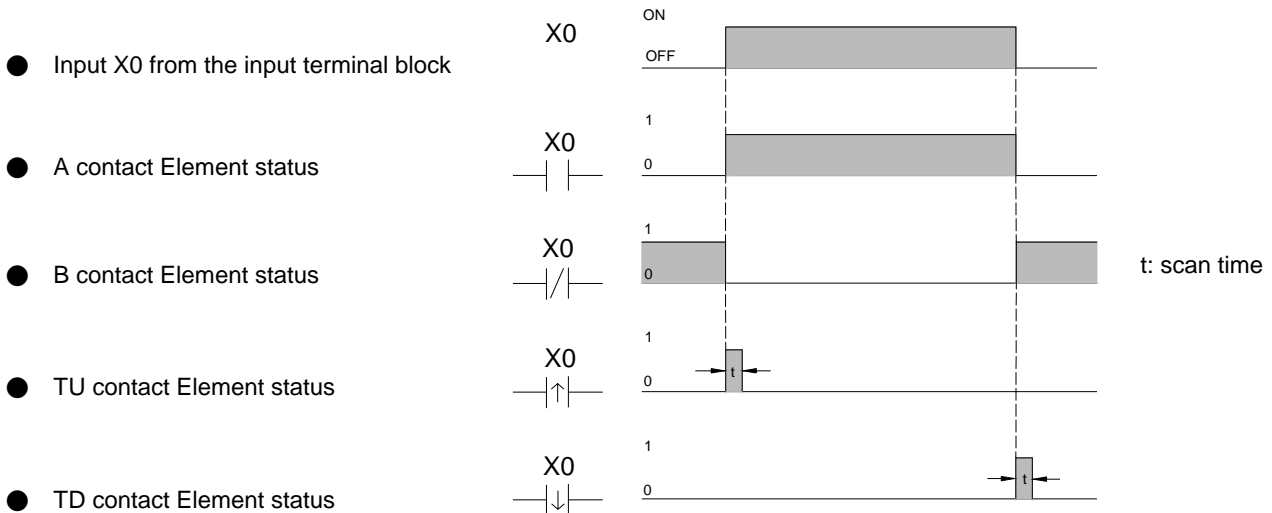
4.1 Valid Operand of Sequential Instructions

Instruction \ Operands Ranges	X	Y	M	SM	S	T	C	TR	OPEN	SHORT
	X0 X255	Y0 Y255	M0 M1911	M1912 M2001	S0 S999	T0 T255	C0 C255	TR0 TR39	—	—
ORG	○	○	○	○	○	○	○		○	○
ORG NOT	○	○	○	○	○	○	○			
ORG TU	○	○	○	○*	○	○	○			
ORG TD	○	○	○	○*	○	○	○			
LD	○	○	○	○	○	○	○	○	○	○
LD NOT	○	○	○	○	○	○	○			
LD TU	○	○	○	○*	○	○	○			
LD TD	○	○	○	○*	○	○	○			
AND	○	○	○	○	○	○	○		○	○
AND NOT	○	○	○	○	○	○	○			
AND TU	○	○	○	○*	○	○	○			
AND TD	○	○	○	○*	○	○	○			
OR	○	○	○	○	○	○	○		○	○
OR NOT	○	○	○	○	○	○	○			
OR TU	○	○	○	○*	○	○	○			
OR TD	○	○	○	○*	○	○	○			
OUT		○	○	○*	○			○		
OUT NOT		○	○	○*	○					
OUT L		○								
ANDLD	—									
ORLD	—									
TU	—									
TD	—									
NOT	—									
OUTS		○	○	○*	○					
OUTR		○	○	○*	○					

※For the relays marked with a  symbol in the special relay table (please refer to section 2.3) is write prohibited. In addition, TU and TD contacts are not supported for those relays as well. The operands marked with a ‘**’ symbol in the table shown above should exclude those special relays.

4.2 Element Description

4.2.1 Characteristics of A,B,TU and TD Contacts

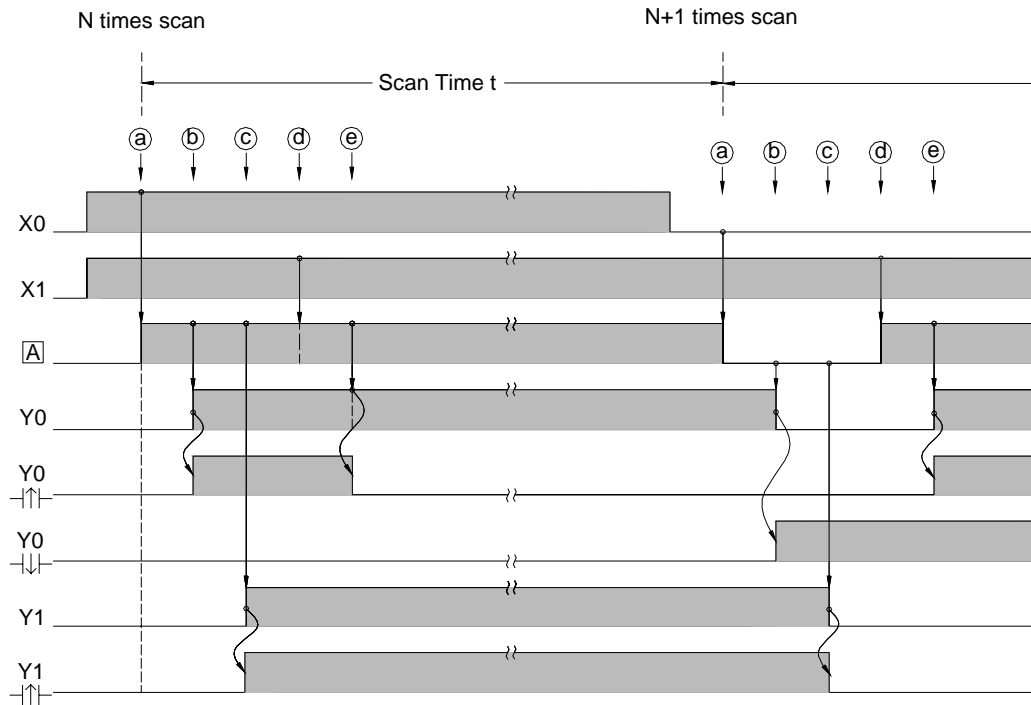


The waveform shown above reveals the function of A, B, TU and TD elements by exercising the external input X0 from OFF to ON then OFF.

- TU (Transition Up): This is the “Transition Up Contact”. Only a rising edge (0→1) of the referenced signal will turn on this element for one scan time.
- TD (Transition Down): This is the “Transition Down Contact”. Only a falling edge (1→0) of the referenced signal will turn on this element for one scan time.
- TU and TD contact will work normally as described above if the change of the status of the valid referenced operands listed in the “Valid Range of the Operand of Sequential instructions” table are not driven by the function instructions.

Remark: For TU(TD) elements which operand is of relay will turn on after the first time the corresponding relay get driven from 0 to 1(1 to 0). When the next time the corresponding relay get driven from 1 to 1(0 to 0) the TD(TU) element will turn OFF. Care should be taken while there is a multiple coil usage situation existed in the ladder program. This situation can be best illustrated at below. In the waveform we can see Y0 TU element only turn on between ⑥ and ⑦ time which only the Y0 TU elements existed between rung 1 and rung 2 can detect the Y0 rising edge, while other Y0 TU elements out side these two ladder rungs will never aware the occurrence of the rising edge. For the relays do not have the multiple coil usage in ladder program, The ON status of corresponding TU or TD element can be sustained for one scan time, but for relays which contrary to above, the turn on time will shorter than 1 scan time as illustrated at below.

Ladder Diagram	Mnemonic code
	<pre> ORG X 0 -----(a) OUT Y 0 -----(b) OUT Y 1 -----(c) ORG X 1 -----(d) OUT Y 0 -----(e) </pre>

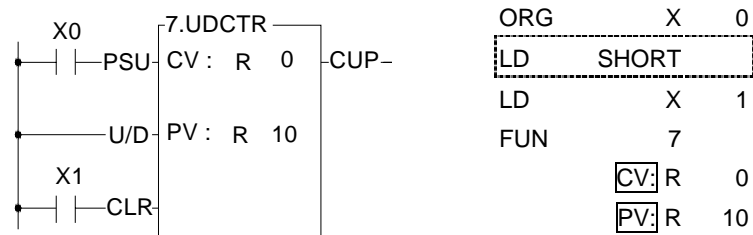


[A]: The internal accumulator of PLC

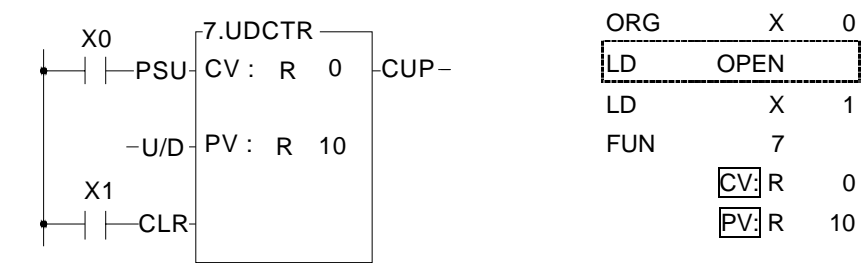
- Besides the TU/TD instructions which can detect the status change of reference operand, FBs-PLC also provides the instructions to detect the change of node status (power flow). For details please refer the descriptions of FUN4 (DIFU) and FUN5 (DIFD) instructions.

4.2.2 OPEN and SHORT Contact

The status of OPEN and SHORT contact are fixed and can't be changed by any ladder instructions. Those two contacts are mainly used in the places of the Ladder Diagram where fixed contact statuses are required, such as the place where the input of an application instruction is used to select the mode. The sample program shown below gives an example of configuring an Up/Down counter (UDCTR) to an Up counter by using the SHORT contact.

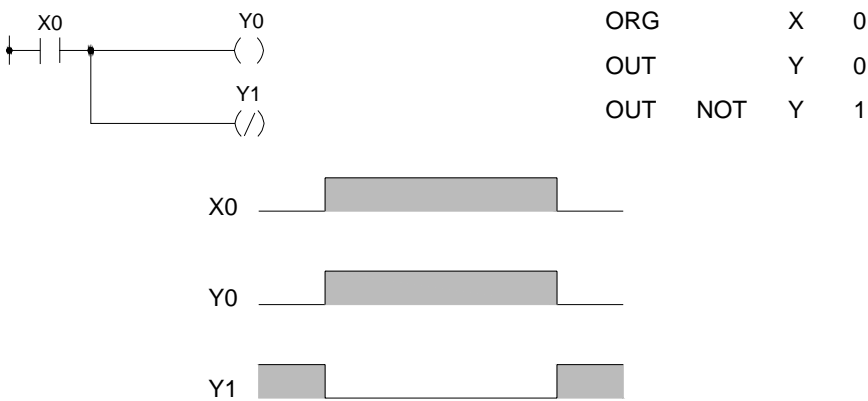


FUN7 is the UDCTR function. While rising edge of CK input occur, FUN7 will count up if the U/D status is 1 or count down if the U/D status is 0. The example shown above, U/D status is fixed at 1 since U/D is directly connected from the origin-line to a SHORT contact, therefore FUN7 becomes an Up counter. On the contrary, if the U/D input of FUN7 is connected with an OPEN contact from the origin-line, the FUN7 becomes a DOWN counter.



4.2.3 Output Coil and Inverse Output Coil

Output Coil writes the node status into an operand specified by the coil instruction. Invert Output Coil writes the complement status of node status into an operand specified by the coil instruction. The characteristics depicts at below.



4.2.4 Retentive Output Coil

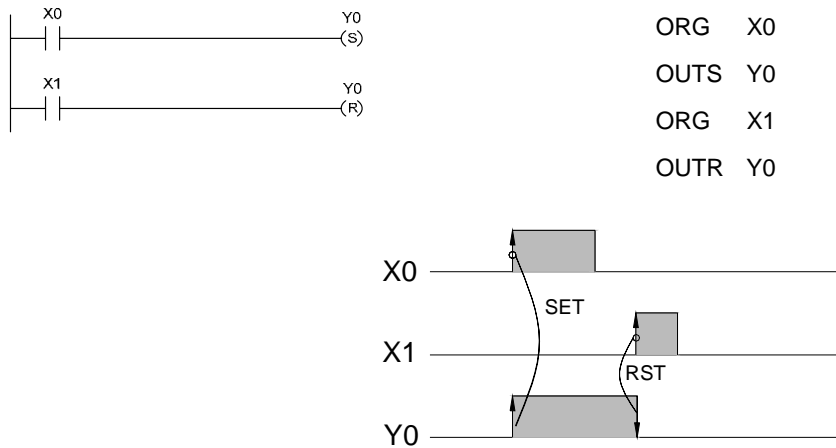
The coil element can be categorized into two types, namely Retentive and Non Retentive. For example, M0~M799 can be specified as the Retentive coils and M800~M1399 can be specified as the Non Retentive coils. One way to categorize the relay type is to divide the relays into groups. Though this method is simple but for the most applications the coils needed to be retentive may be in a random order. FBs-PLC allows user to set the retentive status of coil individually. When input the program with mnemonics instructions, if put an "L" after the OUT instruction can declare this specific relay as retentive output. This can be shown in the diagram below.



From the above example, if turn the X0 "ON" then "OFF", Y0 will keep at "ON". When change the PLC state from RUN to STOP then RUN or turn the power off then on, the Y0 still keep at ON state. But if use the OUT Y0 instruction instead of the OUT L Y0 , Y0 status will be OFF.

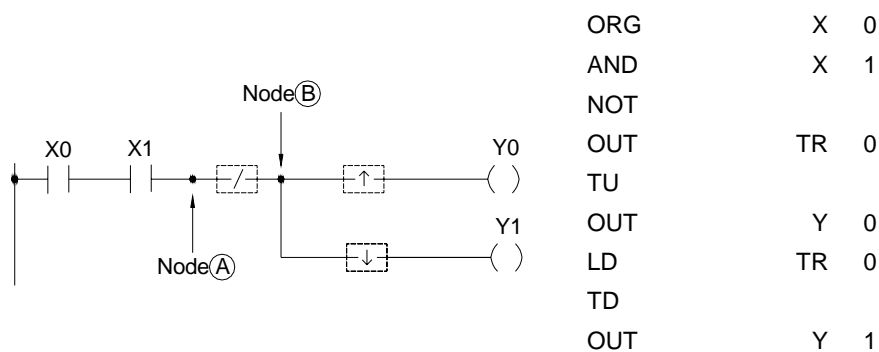
4.2.5 Set Coil and Reset Coil

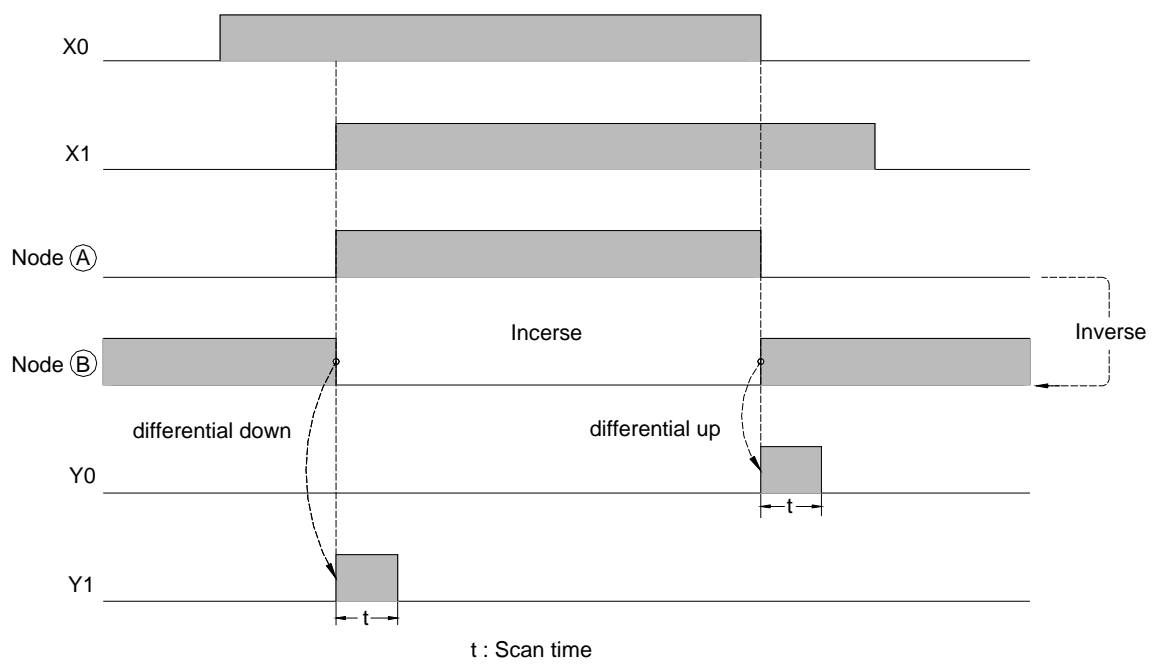
Set Coil writes 1 into an operand specified. Reset Coil writes 0 into an operand specified. The characteristics depicts at below.



4.3 Node Operation Instructions

A node is the connection between elements in a ladder diagram consisting of sequential instruction elements (please refer to Section 1.2). There are four instructions dedicated for node status operation in FBs-PLC. The two instructions, “OUT TR” and “LD TR”, have been discussed in Section 1.6 of this manual. Using the diagram below, the three node operation instructions NOT, TU and TD, are illustrated.

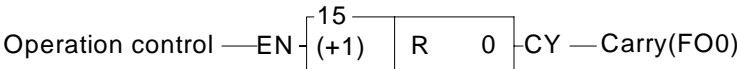
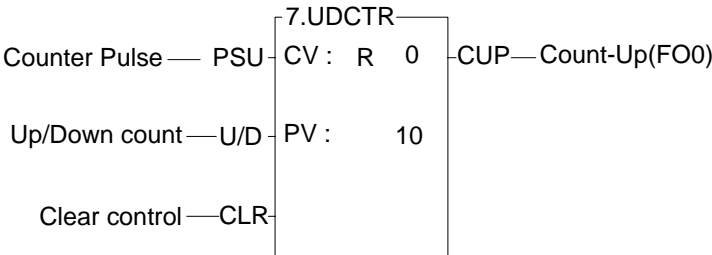




Chapter 5 Description of Function Instructions

5.1 The Format of Function Instructions

In this chapter we will introduce the function instructions of FBs-PLC in details. All the explanations for each function will be divided into four parts including input control, instruction number/name, operand and function output. If use the FP-08 to input the mnemonic instruction, except for the T, C, SET, RST and SFC instructions that can be entered directly by pressing a single key stroke on FP-08, other function instructions must be entered by key in the instruction number rather than the instruction name. An example is shown in below.

Ladder Diagram		FP-08 Mnemonic code
Example 1: Single input instruction 		FUN 15 D: R 0
Example 2: Multiple input instruction 		FUN 7 CV: R 0 PV: 10

Remark : The words inside the hollow box in mnemonic code field are the prompting message from FP-08 such as D:, CV:, and Pr: and are not entered by the user.

5.1.1 Input Control

Except for the seven function instructions that do not have input control, the number of the input control of other FBs-PLC function instructions can be ranged from one to four. Execution of the instructions and operations is dependent on the input control signal or the combinations of the several input control signals. The ladder programming software for FACON PLC - WinProladder can help user to complete the complex design and document works. In the ladder program window we can see all the function instructions were displayed by blocks surrounded with abbreviated words for ease of comprehension, include inputs, outs, function name, and parameter names. As shown in example 2 above, the first input mark "PSU" indicates when the "PSU" input changes from 0 to 1 (rising edge) the counter will be increased or decreased by 1 (depending on the "U/D" status). The second input mark "U/D" with a status of 1 represents the word above slash ("U") and the status 0 represents the word under slash ("D"), that is second input "U/D" states =1, the counter will be increased by 1 when "PSU" input from 0 to 1, and when "U/D"=0, the counter will be decreased by 1. The third input mark "CLR" indicates when this input is 1, the counter will be cleared to 0. Chapter 7 give the descriptions of input control of each function instruction.

Remark: There are total of seven instructions whose input control should be directly connected to the origin-line those are MCE, SKPE, LBL, RTS, RTI, FOR, and NEXT. Please refer to chapter 6 and 7 for more detailed explanations.

All input controls of the function instructions should be connected by the corresponding elements, otherwise a syntax error will occur. As shown in example 3 below, the function instruction FUN7 has three inputs and three elements before FUN7. ORG X0, LD X1 and LD X2 corresponds to the first input PSU, second input U/D and third input CLR.

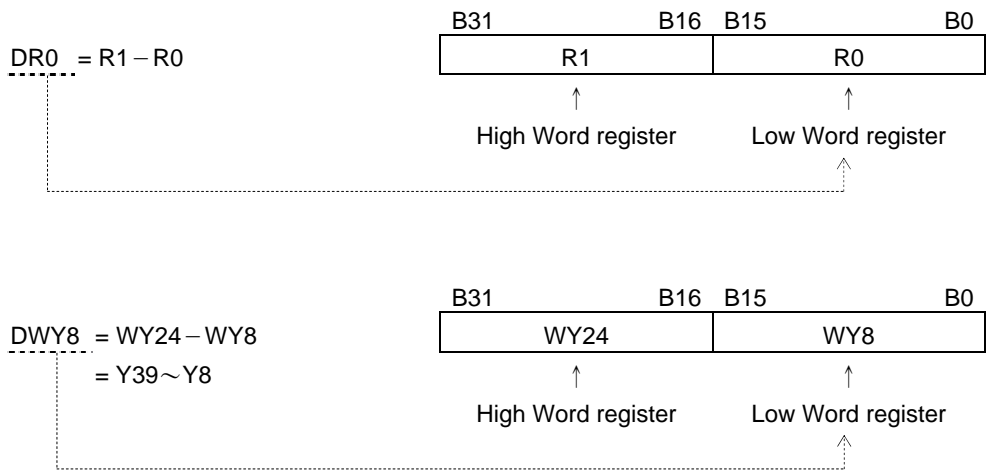
Example 3:

Ladder Diagram	FP-08 Mnemonic code
	<pre> ORG X0 LD X1 LD X2 FUN 7 CV: R 0 PV: 10 </pre> <p>FUN7 need three elements because it has three inputs</p>

5.1.2 Instruction Number and Derivative Instructions

As mentioned before, except for the nine instructions that can be entered using the dedicated keys on the keyboard, other function instructions must be entered using the "instruction number". Follow the instruction number there are postfixes **D**, **P**, **D P** can be added which can derive three additional function instructions.

D: Indicates a Double Word (32-bit). The 16-bit word is the basic unit of the registers in FBs-PLC. The data length of R, T and C (except C200~C255) registers are 16-bit. If a register with 32-bit data length is required, then it is necessary to combine two consecutive 16-bit registers together such as R1-R0, R3-R2 etc. and those registers are represented by prefix a D letter before register name such as DR0 represents R1-R0 and DR2 represents R3-R2. If you enter DR0 or DWY8 in the monitor mode of FP-08, then a 32-bit long value (R1-R0 or WY24-WY8) will be displayed.

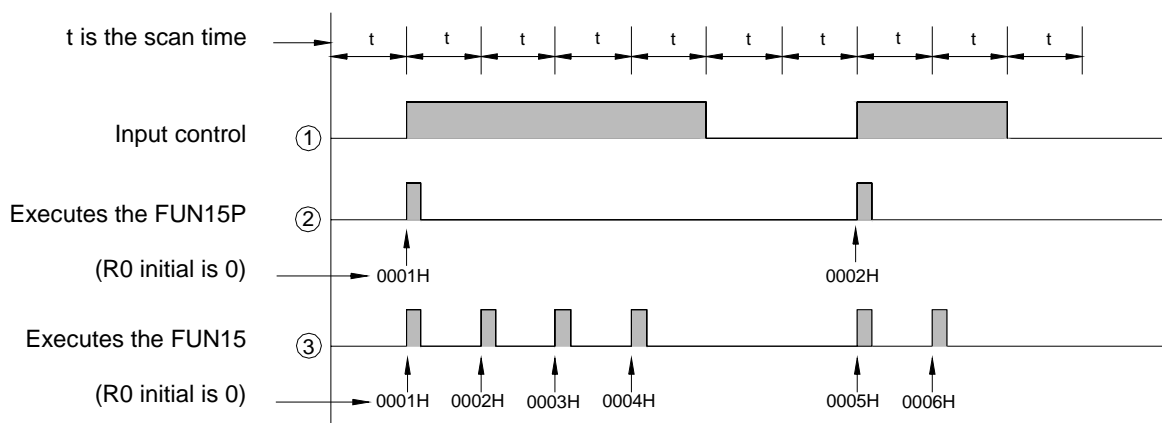


Remark: In order to differentiate between 16-bit and 32-bit instructions while using the ladder diagram and mnemonic code, we add the postfix letter D after the "Instruction number" to represent 32-bit instructions and the size of their operand are 32-bit as shown in example 4 on P.6-6. The instruction FUN 11D has a postfix letter D, therefore the source and destination operands need to prefix a letter D as well, such as the augend Sa : R0 is actually Sa=DR0=R1-R0 and Sb=DR2=R3-R2. Please also pay special attention to the length of the other operands except source and destination are only one word whether 16-bit or 32-bit instructions are used.

P: indicates the pulse mode instruction. The instruction will be executed when the status of input control changes from 0 to 1 (rising edge). As shown in example 1, if a postfix letter P is added to the instruction (FUN 15P), the instruction FUN 15P will only be executed when the status of input control signal changes from 0 to 1. The execution of the instruction is in level mode if it does not have a P postfix, this means the instruction will be executed for every scan until the status of input control changes from 1 to 0. In this operation manual, an example of the operation statement of a function instruction is shown below.

● When the operation control "EN" =1 or (**P** instruction) from 0→1,

The first one indicates the execution requirement for non-P instruction (level mode) and the second one indicates the execution requirement for **P** instruction (pulse mode). The following waveform shows the result (R0) of FUN15 and FUN15P under the same input condition.



DP: Indicates the instruction is a 32-bit instruction operating with pulse mode.

Remark: **P** instruction is much more time saving than level instruction in program scanning, So user should use **P** instruction as much as possible.

5.1.3 Operand

The operand is used for data reference and storage. The data of source (S) operand are only for reference and will not be changed with the execution of the instruction. The destination (D) operand is used to store the result of operation and its data may be changed after the execution of the instruction. The following table illustrates the names and functions of FATEK PLC function instruction's operands and types of contacts, coils, or registers that can be used as an operand.

■ The names and functions of the major operands:

Abbreviation	Name	Descriptions
S	Source	The data of source (S) operand are only for reading and reference and will not be changed with the execution of the instruction. If there are more than one source operands, each operand will be identified by the footnote such as Sa and Sb.
D	Destination	The destination (D) operand is used to store the result of operation. The original data will be changed after operation. Only the coils and registers which are not write prohibited can be the destination operand.
L	Length	Indicates the data size or the length of the table, usually are constants.
N	Number	A constant most often used as numbers and times. If there are more than one constant, each constant will be identified by the footnotes such as Na, Nb, Ns, Nd, etc..
Pr	Pointer	Used to point to a specific a block of data or a specific data or register in a table. Generally the Pr value can be varied, therefore cannot be constant or input register.
CV	Current value	Used in T and C instruction to store the current value of T or C
PV	Set value	Used in T and C instructions for reference and comparison
T	Table	A combination of a set of consecutive registers forms a table. The basic operation units are word and double word. If there is more than one table, each table will be identified by footnotes such as Ta, Tb, Ts and Td etc..
M	Matrix	A combination of a set of consecutive registers forms a matrix. The basic operation unit is bit. If there is more than one matrix, each matrix will be identified by footnotes such as Ma, Mb, Ms and Md etc..

Besides the major operands mentioned above, there are other operands which are used for certain special purposes such as the operand Fr for frequency, ST for stack, QU for Queue etc.. Please refer to the instruction descriptions for more details.

■ The types of the operand and their range: The types of operand for the function instructions are discrete, register and constant.

a) Discrete operand :

There are total five function instructions that reference the discrete operand, namely SET, RST, DIFU, DIFD and TOGG. Those five instructions can only be used for operations of Y△△△(external output), M△△△△(internal and special) and S△△△(step) relays. The table shown below indicates the operands and ranges of the five function instructions.

Range	Y	M	SM	S
Ope- rand	Y0 Y255	M0 M1911	M1912 M2001	S0 S999
D	○	○	○*	○

Symbol "O" indicates the D (Destination operand) can use this type of coils as operands. The "*" sign above the "O" shown in SM column indicates that should exclude the write prohibited relays as operands. Please refer to page 2-3 for introduction of the special relays.

b) Register operand :

The major operand for function instructions is register operand. There are two types of register operands: the native registers which already is of Words or Double Words data such as R, T, C. The other is derivative registers (WX, WY, WM, WS) which are formed by discrete bits. The types of registers that can be used as

instruction operands and their ranges are all listed in the following table:

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number	V · Z P0~P9
	S	○	○	○	○	○	○	○	○	○	○*	○	○	○
D		○	○	○	○	○	○		○	○*	○*	○		○
⋮														

The "○" symbol in the table indicates can apply this kind of data as operand. The "○*" symbol indicates can apply this kind of data except the write prohibited registers as operand. To learn more about write prohibited registers please refer to page 2-8 for introduction of the special register.

When R5000~R8071 are not set to be read only registers, can used as normal registers (read, and write)

- Remark 1: The registers with a prefix W, such as WX, WY, WM and WS are formed by 16 bits. For example, WX0 means the register is formed by X0(bit 0)~X15(bit 15). WY144 means the register is formed by Y144(bit 0)~Y159(bit 15). Please note that the discrete number must be the multiple of 8 such as 0, 8, 16, 24....
- Remark 2: The last register (Word) in a table can not be represented as a 32-bit operand in the function because 2 Words are required for a 32-bit operand.
- Remark 3: TMR (T0~T255) and CTR (C0~C255) are the registers of timers and counters respectively. Although they can be used as general registers, they also complicate the systems and make debugging more difficult. Therefore you should avoid writing anything into the TMR or CTR registers.
- Remark 4: T0~T255 and C0~C199 are 16-bit register. But C200~C255 are 32-bit register, therefore can't be used as 16-bit operands.
- Remark 5: Apart from being directly appointed by register's number (address) as the foregoing discussions, the register's operand in the range of R0~R8071 can be combined with pointer register V · Z or P0~P9 to make indirect addressing. Please refer to the example in the next section (Section 5.2) for the description of using pointer register (XR) to make indirect addressing.

c) Constant operands :

The range of 16-bit constant is between -32768~32767. The range of 32-bit constant is between -2147483648~2147483647. The constant for several function instructions can only be a positive constant. The range of 16-bit and 32-bit constants are listed in the table shown below.

Classification	Range
16-bit signed number	-32768~32767
16-bit un-signed number	0~32767
32-bit signed number	-2147483648~2147483647
32-bit un-signed number	0~2147483647
16/32-bit signed number	-32768~32767 or -2147483648~2147483647
16/32-bit un-signed number	0~32767 or 0~2147483647

It is possible that the length and size of a specific operand, such as L, bit size, N etc., are different, and the differences are all directly marked at the operand column. Please refer to the explanations of function instructions.

5.1.4 Functions Output (FO)

The “Function Output” (FO) is used to indicate the operation result of the function instruction. Like control input, each function outputs shown in the screen of programming software are all attached with a word which comes from the abbreviation of the output functionality. Such as CY derived from CarrY. The maximum number of function outputs is 4 and those are denoted as FO0, FO1, FO2, FO3 respectively. The FO status must be taken out by FO instruction (there is a FO special key on FP-08 program writing device). The unused FO may be left without connecting to any elements, such as FO1 (CY) shown in Example 4 below.

Example 4 :

Ladder Diagram	Mnemonic Codes
	<pre> ORG X 0 FUN 11D [Sa:] R 0 [Sb:] R 2 [D:] R 4 FO 0 OUT Y 0 FO 2 OUT Y 1 </pre>

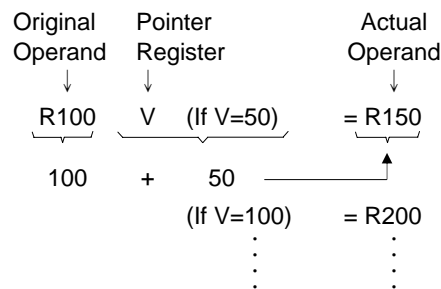
When M1919=0, the FO status will only be updated if the instruction is executed. It will keep the same status until a new FO status is generated after the instruction is executed again (memory keeping).

When M1919=1, the FO status will be reset to 0 (no memory keeping) if the instruction is not executed.

5.2 Use Index Register(XR) for Indirect Addressing

In the FBs-PLC function instructions, there are some operands that can be combined with pointer register (V、Z、P0~P9) to make indirect addressing (will be shown in the operand table if it applicable). However, only the registers in the range R0~R8071 can be combined with an pointer register to perform indirect addressing (other operands such as discrete, constant and D0~D3071 cannot be used for indirect addressing).

There are twelve pointer registers XR (V、Z、P0~P9). The V register in fact is the R4164 of special registers (R3840~R4167), the Z register is the R4165 and the P0~P9 register is the (D4080~D4089). The actual addressed register by index addressing is just offset the original operand with the content of the index register.



As shown in the above diagram, you only need to change the V value to change the operand address. After combining the index addressing with the FBs-PLC function instructions, a powerful and highly efficient control application can be achieved by using very simple instructions. Using the program shown in the diagram below as an example, you only need to use a block move instruction (BT_M) to achieve a dynamic block data display, such as a parking management system.

Index Register(P0~P9) Introduction

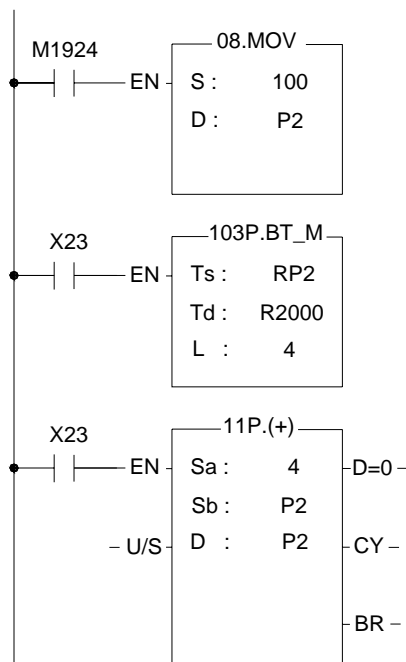
In indirect addressing application, Rxxxx register can combine V、Z & P0~P9 for index addressing; Dxxxx register can't combine V、Z for index addressing, but P0~P9 are allowed.

When V、Z index register being combined with the Rxxxx register,

for example, R0 with V、Z, the instruction format is R0V(where V=100, it means R100) or R0Z(where Z=500, it means R500); when P0~P9 index register being combined with the Rxxxx register, the instruction format is RPn (n=0~9) or RPmPn (m,n=0~9), for example RP5 (where P5=100, it means R100) or RP0P1(where P0= 100, P1=50, it means150).

When P0~P9 index register being combined with the Dxxxx register, the instruction format is DPn (n=0~9) or DPmPn (m,n=0~9), for example DP3 (where P3=10, it means D10) or DP4P5 (where P4=100, P5=1, it means D101).

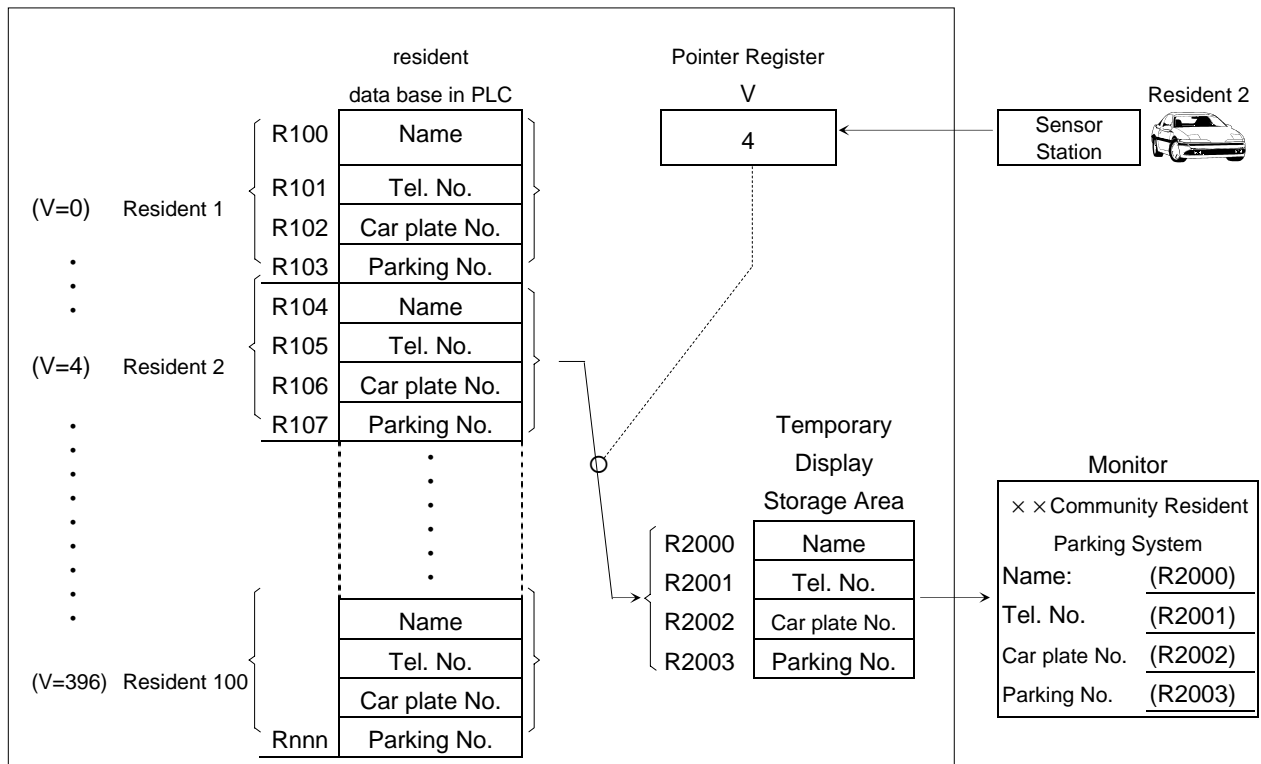
It can combine both P0~P9 index register, for example P2=20, P3=30, when Rxxxx or Dxxxx register combines both index register, RP2P3 will point to R50, DP2P3 will point to D50, it means the summation of both index register for indirect addressing.



1. Index register P2=100 while power up or first run.
2. When X23 changes from 0→1, FUN103 will perform the table movement, the source starts from R100 (P2=100), the destination starts from R2000, the amount is 4. Copying the content of R100~R103 for R2000~R2003 at first execution, copying the content of R104~R107 for R2000~R2003 at second execution...
3. Increasing the P2 index register by 4 to point to next 4

Indirect addressing program example

Ladder Diagram	Mnemonic Codes
	<pre> ORG SHORT FUN 103 [Ts:] R100V [Td:] R2000 [L:] 4 </pre>



Description

Suppose that there are 100 resident parking spaces available in a parking management system for community residents. Each resident has a set of basic information including name, telephone number, number plate and parking number, that occupy four consecutive PLC registers as shown in the above diagram. A total of 400 registers (R100~R499) are occupied. Each resident is given a card with a unique card number (the number is 0 for resident 1, 4 for resident 2 etc..) for the sensing pass of the main entrance and parking lot. The card number will be sensed by the PLC and stored into the pointer register “V”. The attendant’s monitor (LCD or CRT) will only display the data grasped by R2001~R2003 in the PLC. For example, the card of residence 2 with the card number 4 is sensed, then the register V=4 and the PLC will immediately move the data in R104~R107 to the temporary display storage area (R2000~R2003). Hence, the attendant’s monitor can display the data of residence 2 as soon as its card is sensed.

⚠ Warning

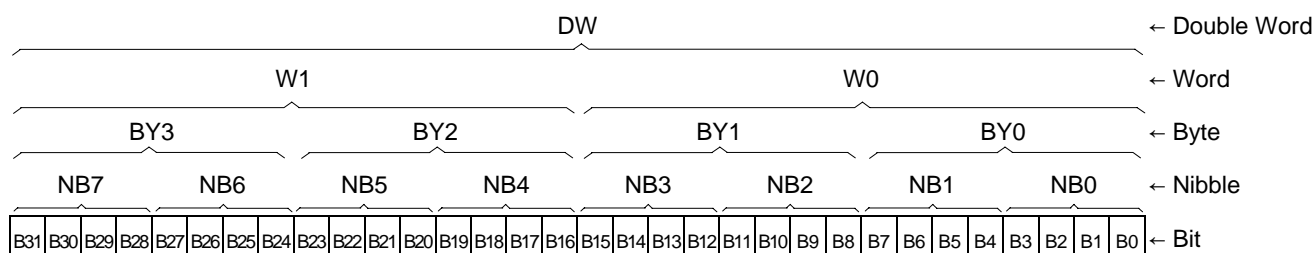
1. Although using pointer register for indirect addressing application is powerful and flexible, but changing the V and Z values freely and carelessly may cause great damages with erroneous writing to the normal data areas. The user should take special caution during operation.
2. In the data register range that can be used for indirect addressing application (R0~R8071), the 328 registers R3840~R4167 (i.e. IR, OR and SR) are important registers reserved for system or I/O usage. Writing at-will to these registers may cause system or I/O errors and may result in a major disaster. Due to the fact that users may not easily detect or control the flexible register address changes made by the V and Z values, FBs-PLC will automatically check if the destination address is in the R3840~R4067 range. If it is, the write operation will not be executed and the M1969 flag "Illegal write of Indirect addressing" will be set as 1. In case it is necessary to write to the registers R3840~R4067, please use the direct addressing.

5.3 Numbering System

5.3.1 Binary Code and Related Terminologies

Binary is the basic numbering system of digital computer. Since the PLC operates with discrete ON/OFF values, it is natural to use binary codes. The following terminologies should be fully understood before go to further topic of numbering system.

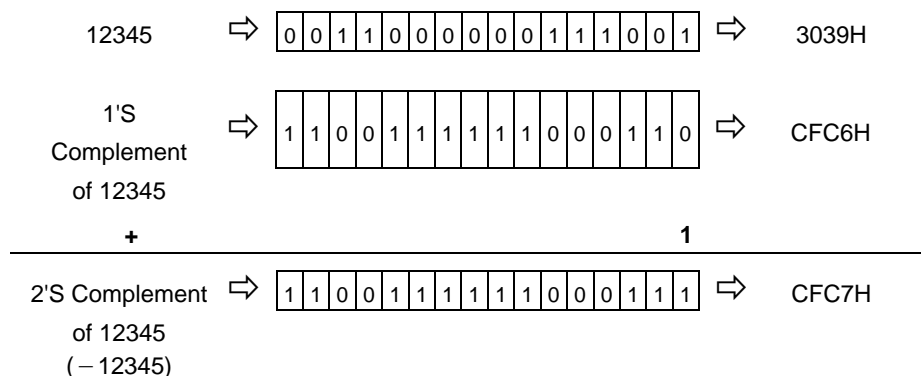
- Bit: (Abbreviated as B, such as B0, B1, and so on) It is the most basic unit of binary value. The status of bit is either "1" or "0".
- Nibble: (Abbreviated as NB, such as NB0, NB1, and so on) It is formed by four consecutive bits (e.g. B3~B0) and can be used to represent a decimal number 0~9 or a hexadecimal number 0~F.
- Byte: (Abbreviated as BY, such as BY0, BY1, and so on) It is formed by two consecutive nibbles (or 8 bits, such as B7~B0) and can be used to represent a 2-digit hexadecimal number 00~FF.
- Word: (Abbreviated as W, such as W0, W1, and so on) It is formed by two consecutive bytes (or 16 bits, such as B15~B0) and can be used to represent a 4-digit hexadecimal number 0000~FFFF.
- Double Word: (Abbreviated as DW, such as DW0, DW1, and so on) It is formed by two consecutive words (or 32 bits, such as B31~B0) and can be used to represent an 8-digit hexadecimal number 00000000~FFFFFFFF.



- Floating Point Number: It is also formed by two consecutive words. The Floating Point Number can expressed the maximum range is $\pm(1.8 \times 10^{-38} \sim 3.4 \times 10^{38})$. For the details, Please refer to section 5.3.6 for explanation.

5.3.5 Representation of Negative Number (Beginners should skip this section)

As prior discussion, when the MSB is 1, the number will be a negative number. The FBs-PLC negative numbers are represented by 2'S Complement, i.e. to invert all the bits (B15~B0 or B31~B0) of its equivalent positive number (The so-called 1'S Complement is to change the bits equal 1 to 0 and the bits equal 0 to 1) then add 1. In the above example, the positive number is 12345. The calculation of its 2'S Complement (i.e. -12345) is described below:



5.3.6 Representation of Floating Point Number (Beginners should skip this section)

The format of floating point number of FATEK-PLC follows the IEEE-754 standard, which use a double word for storage and can be expressed as follow:

floating point number = sign + Exponent + Mantissa

Sign	Exponent	Mantissa
b ₃₁	b ₃₀ ~ b ₂₃	b ₂₂ ~ b ₀
1 bit	8 bits	23 bits

32 bits

- ▲ If the sign bit is 0 the number is positive, if the sign bit is 1 the number is negative.
- ▲ The exponent is denoted as 8-bit excess 127.
- ▲ The mantissa is 23-bit with radix 2. A normalized mantissa always starts with a bit 1, followed by the radix point, followed by the rest of the mantissa. The leading bit 1, which is always present in a normalized mantissa, is implicit and is not represented.

- The Conversion rule of Integer to floating is :

$$N = (-1)^S * 2^{(E-127)} * (1.M) \quad 0 < E < 255$$

For example :

$$(1). 1 = (-1)^0 * 2^{(01111111)} * (1.000\ldots\ldots 0)$$

The sign is represented by 0, the exponent's code in excess 127 is 127 = 01111111, and the significant bit is 1, resulting in the mantissa being all 0's. The simple precision IEEE 754 representation of 1, is thus :

$$\begin{aligned} \text{Code}(1) &= \begin{array}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|} \hline 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & \cdots & 0 & 0 & 0 \\ \hline s & e & e & e & e & e & e & e & e & m & m & m & m & m & m & \cdots & m & m & m \\ \hline \end{array} \\ &= 3F800000H \end{aligned}$$

$$(2). 0.5 = (-1)^0 * 2^{(01111110)} * (1.000\ldots\ldots 0)$$

Code(0.5) =

0	0	1	1	1	1	1	1	0	0	0	0	0	0.....0	0	0
s	e	e	e	e	e	e	e	e	m	m	m	m	m m..... m	m	m

= 3F000000H

The sign is represented by 1, the exponent's code in excess 127 is $135 - 127 = 10000111$, and the significant bit is 1, resulting in the mantissa is 1111010000100000000000. The simple precision IEEE 754 representation of -500.125, is thus :

Code(-500.125) =

1	1	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0	0	1	0	0	0	00.....0	0
s	e	e	e	e	e	e	e	e	e	m	m	m	m	m	m	m	m	m	m	m	m	m	mm.....m	m

= C3FA1000H

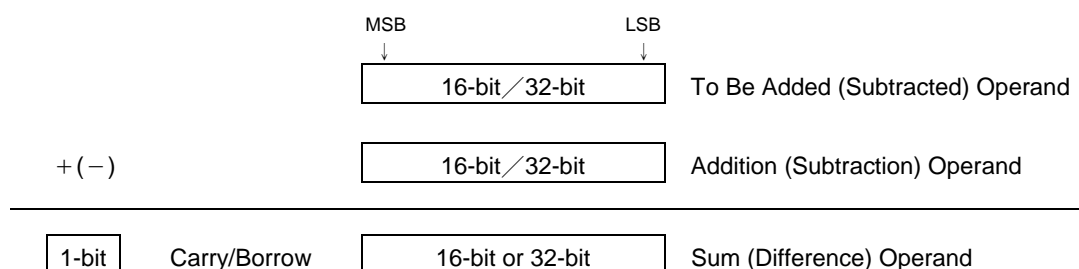
5.4 Overflow and Underflow of Increment (+1) or Decrement (-1) (Beginners should skip this section)

5-12

<div> <div>Increase (Decrease) Result</div> <div>Overflow/ Underflow</div> </div>	16-bit Operand	32-bit Operand
Increase	<div> <div> <div>– 32767</div> <div>– 32768</div> <div>OVF=1</div> <div>32767</div> <div>32766</div> <div>32765</div> </div> </div>	<div> <div> <div>– 2147483646</div> <div>– 2147483647</div> <div>OVF=1</div> <div>– 2147483648</div> <div>2147483647</div> <div>2147483646</div> </div> </div>
Decrease	<div> <div> <div>– 32767</div> <div>– 32768</div> <div>UDF=1</div> <div>32767</div> <div>32766</div> <div>32765</div> </div> </div>	<div> <div> <div>– 2147483647</div> <div>– 2147483648</div> <div>UDF=1</div> <div>2147483647</div> <div>2147483646</div> <div>2147483645</div> </div> </div>

5.5 Carry and Borrow in Addition/Subtraction

Overflow/Underflow takes place when the operation of increment/decrement causes the value of the operand to exceed the positive/negative limit that can be represented in the PLC, consequently a flag of overflow/underflow is introduced. Carry/Borrow flag is different from overflow/underflow. At first, there must be two operands making addition (subtraction) where a sum (difference) and a flag of carry/borrow will be obtained. Since the number of bits of the numbers to be added (subtracted), to add (subtract) and of sum (difference) are the same (either 16-bit or 32-bit), the result of addition (subtraction) may cause the value of sum (difference) to exceed 16-bit or 32-bit. Therefore, it is necessary to use carry/borrow flag to be in coordination with the sum (difference) operand to represent the actual value. The carry flag is set when the addition (subtraction) result exceeds the positive limit (32767 or 2147483647) of the sum (difference) operand. The borrow flag is set when addition (subtraction) result exceeds the negative limit (– 32768 or – 2147483648) of the sum (difference) operand. Hence, the actual result after addition (subtraction) is equal to the carry/borrow plus the value of the sum (difference) operand. The FO of FBs-PLC addition/subtraction instruction has both carry and borrow flag outputs for obtaining the actual result.



While all FBs-PLC numerical operations use 2'S Complement, the representation of the negative value of the sum (difference) obtained from addition (subtraction) is different from the usual negative number representation. When the operation result is a negative value, 0 can never appear in the MSB of the sum (difference) operand. The carry flag represents the positive value 32768 (2147483648) and the borrow flag represents the negative value -32768 (-2147483648).

			MSB															LSB			
C=1	B=0	Z=0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	32769	Positive Value	
C=1	B=0	Z=0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	32768		
C=0	B=0	Z=0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	32767		
C=0	B=0	Z=0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	32766		
C=0	B=0	Z=0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	32765		
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C=0	B=0	Z=0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	2		
C=0	B=0	Z=0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1		
C=0	B=0	Z=1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
C=0	B=0	Z=0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-1		
C=0	B=0	Z=0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	-2			
			.																	.	Negative Value
			.																	.	
			.																	.	
			.																	.	
			.																	.	
C=0	B=0	Z=0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	-32766		
C=0	B=0	Z=0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	-32767			
C=0	B=0	Z=0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-32768			
C=0	B=1	Z=0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-32769			
C=0	B=1	Z=0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	-32770			
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Chapter 6 Basic Function Instruction

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Basic Function Instruction

T	TIMER												T																																																																					
Symbol																																																																																		
													Operand																																																																					
													Ladder symbol																																																																					
													Tn: Timer Number																																																																					
													PV: Preset value of the timer.																																																																					
													TB: Time Base (0.01S, 0.1S, 1S)																																																																					
<table><tr><td>Range</td><td>WX</td><td>WY</td><td>WM</td><td>WS</td><td>TMR</td><td>CTR</td><td>HR</td><td>IR</td><td>OR</td><td>SR</td><td>ROR</td><td>DR</td><td>K</td></tr><tr><td rowspan="2">Ope- rand</td><td>WX0</td><td>WY0</td><td>WM0</td><td>WS0</td><td>T0</td><td>C0</td><td>R0</td><td>R3840</td><td>R3904</td><td>R3968</td><td>R5000</td><td>D0</td><td>0</td></tr><tr><td>WX240</td><td>WY240</td><td>WM1896</td><td>WS984</td><td>T255</td><td>C255</td><td>R3839</td><td>R3903</td><td>R3967</td><td>R4167</td><td>R8071</td><td>D4095</td><td>32767</td></tr><tr><td>Tn</td><td></td><td></td><td></td><td></td><td>○</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>PV</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td></tr></table>														Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	0	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	32767	Tn					○									PV	○	○	○	○	○	○	○	○	○	○	○	○	○
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K																																																																					
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PV	○	○	○	○	○	○	○	○	○	○	○	○	○																																																																					
<ul style="list-style-type: none">● The total number of timers is 256 (T0~T255) with three different time bases, 0.01S, 0.1S and 1S.The default number and allocation of timers is shown as below (Can be adjusted according to user's actual requirements by the "Configuration" function):<div>T0~T49 : 0.01S timer (default as 0.00~327.67S) ◦</div><div>T50~T199 : 0.1S timer (default as 0.0~3276.7S) ◦</div><div>T200~T255 : 1S timer (default as 0~32767S) ◦</div>● FBs-PLC programming tool will lookup the timer's time base automatically according to the "Memory Configuration" after the timer number is keyed in. Timer's time = Time base x Preset value. In the example 1 below, the time base T0 = 0.01S and the PV value = 1000, therefore the T0 timer's time = 0.01S x 1000 = 10.00S.● If PV is a register, then Timer's time = Time base x register content. Therefore, you only need to change the register content to change the timer's time. Please refer to Example 2.※ The maximum error of a timer is a time base plus a scan time. In order to reduce the timing error in the application, please use the timer with a smaller time base.																																																																																		
Description	<ul style="list-style-type: none">● When the time control "EN" is 1, the timer will start timing (the current value will accumulate from 0) until "Time Up" (i.e. $CV \geq PV$), then the Tn contact and TUP (FO0) will change to 1. As long as the timer control "EN" input is kept as 1, even the CV of Tn has reached or exceeded the PV, the CV of the timer will continue accumulating (with M1957 = 0) until it reaches the maximum limit (32767). The Tn contact status and flag will remain as 1 when $CV \geq PV$, unless the "EN" input is 0. When "EN" input is 0, the CV of Tn will be reset to 0 immediately and the Tn contact and "Time Up" flag TUP will also change to 0 (please refer to the diagram ① below).● If the FBs-PLC OS version is higher than V3.0 (inclusive), the M1957 can be set to 1 so the CV will not accumulate further after "Time Up" and stops at the PV value. The default value of the M1957 is 0, therefore the status of M1957 can be set before executing any timer instruction in the program to individually set the timer CV to continue accumulating or stop at the PV after "Time Up" (please refer to the diagram ② below).																																																																																	

T	TIMER		T
Example 1	Constant preset value		
<div><div><div><div>Ladder diagram</div><div><div><div><div>X1</div><div> </div><div> </div><div>EN</div></div><div><div><div>.01S</div><div>T0</div><div>1000</div></div><div>TUP</div><div>Y0</div></div></div><div><div>P</div><div>SET</div><div>M1957</div></div><div><div>X1</div><div> </div><div> </div><div>EN</div></div><div><div><div>.01S</div><div>T1</div><div>1000</div></div><div>TUP</div><div></div></div></div><div><div>An example of taking "Time-Up" signal directly from FO0.</div></div><div><div><div>ORG</div><div>X</div><div>1</div><div>ENT</div></div><div><div>T</div><div>0</div><div>OPEN</div><div>HEX</div></div><div><div>1</div><div>SHORT</div><div>0</div><div>OPEN</div><div>0</div><div>OPEN</div><div>0</div><div>OPEN</div><div>ENT</div></div><div><div>FO</div><div>NOT</div><div>0</div><div>OPEN</div><div>ENT</div></div><div><div>OUT</div><div>Y</div><div>0</div><div>OPEN</div><div>ENT</div></div><div><div>ORG</div><div>1</div><div>SHORT</div><div>ENT</div></div><div><div>SET</div><div>RST</div><div>M</div><div>1</div><div>SHORT</div><div>9</div><div>5</div><div>7</div><div>ENT</div></div><div><div>ORG</div><div>X</div><div>1</div><div>SHORT</div><div>ENT</div></div><div><div>T</div><div>1</div><div>SHORT</div><div>HEX</div></div><div><div>1</div><div>SHORT</div><div>0</div><div>OPEN</div><div>0</div><div>OPEN</div><div>0</div><div>OPEN</div><div>ENT</div></div></div><div><div>ORG</div><div>X</div><div>1</div><div>T0</div><div>PV:</div><div>1000</div><div>FO</div><div>0</div><div>OUT</div><div>Y</div><div>0</div><div>ORG</div><div>SHORT</div><div>SET</div><div>M</div><div>1957</div><div>ORG</div><div>X</div><div>1</div><div>T1</div><div>PV:</div><div>1000</div></div></div></div></div>			
<div><div><div><div>①</div><div>M1957=0</div><div>(Defaulted)</div></div><div><div>②</div><div>M1957=1</div></div></div><div><div><div>X1</div><div>327.67S</div><div>32767</div><div>10.0S</div><div>1000</div><div>0</div><div>T0 (CV)</div><div>Y0 or T0</div><div>1000</div><div>0</div><div>T1 (CV)</div><div>T1</div><div>Time Start</div><div>Time-Up</div><div>CV</div></div></div></div>			
Example 2	Variable PV		
<p>The preset value (PV) shown in example 1 is a constant which is equal to 1000. This value is fixed and can not be changed once programmed. In many circumstances, the preset time of the timers needs to be varied while PLC running. In order to change the preset time of a timer, can first use a register as the PV operand (R or WX, WY...) and then the preset time can be varied by changing the register content. As shown in this example, if set R0 to 100, then T becomes a 10S Timer, and hence if set R0 to 200, then T becomes a 20S Timer.</p>			

Basic Function Instruction

T	TIMER		T
<div><div>Ladder diagram</div><div><p>An example of applying the "time-up" status by using the T50 contact.</p></div></div>	<div><div>Key operations</div><div><div><div>ORG</div><div>X^U</div><div>1^E SHORT</div><div>ENT</div></div><div><div>T^V</div><div>5^J</div><div>0[•] OPEN</div><div>HEX ⇨</div></div><div><div>R^D</div><div>0[•] OPEN</div><div>ENT</div></div><div><div>ORG</div><div>T^V</div><div>5^J</div><div>0[•] OPEN</div><div>ENT</div></div><div><div>OUT</div><div>Y^L</div><div>0[•] OPEN</div><div>ENT</div></div></div></div>	<div><div>Mnemonic code</div><div><div>ORG</div><div>X</div><div>1</div></div><div><div>T</div><div>50</div><div>PV:</div><div>R</div><div>0</div></div><div><div>ORG</div><div>T</div><div>50</div></div><div><div>OUT</div><div>Y</div><div>0</div></div></div>	
<div><div><p>Timing diagram illustrating the timer's operation:</p><ul style="list-style-type: none">X1: Input pulse.T50 0 (current value): Ramp signal from 0 to 200.① When R0=100 ⇒ Y0: Output Y0 is set to 1 at 10.0S.② When R0=200 ⇒ Y0: Output Y0 is set to 1 at 20.0S.Time Start, ① Time-Up, ② Time-Up: Markers for the timer's start and time-up events.</div></div> <div><div>Remark:</div><div>If the preset value of the timer is equal to 0, then the timer's contact status and FO0 (TUP) become 1 ("EN" input must be at 1) immediately after the PLC finishes its first scan because "Time-Up" has occurred. (TUP) stays at 1 until "EN" input changes to 0.</div></div>			

C	COUNTER (16-Bit: C0~C199 , 32-Bit: C200~C255)												C																																																						
Symbol																																																																			
<div><div><div><div><div></div><div>Cn</div><div>PV : <div></div></div></div><div>Clock — PLS</div><div>CUP — Count-UP(FO0)</div><div>Clear control — CLR</div></div><div><div><div></div><div>Cn: The Counter number</div><div>PV: Preset value</div></div></div></div></div>																																																																			
<table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th></tr><tr><td rowspan="2">Ope- rand</td><td>WX0 WX240</td><td>WY0 WY240</td><td>WM0 WM1896</td><td>WS0 WS984</td><td>T0 T255</td><td>C0 C255</td><td>R0 R3839</td><td>R3840 R3903</td><td>R3904 R3967</td><td>R3968 R4167</td><td>R5000 R8071</td><td>D0 D4095</td><td>0 2147483647</td></tr><tr><td>Cn</td><td></td><td></td><td></td><td></td><td>○</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>PV</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td></tr></table>													Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	0 2147483647	Cn					○								PV	○	○	○	○	○	○	○	○	○	○	○	○	○
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K																																																						
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	Cn					○																																																													
PV	○	○	○	○	○	○	○	○	○	○	○	○	○																																																						
<div><div><div><div><div></div><div>There are total 200 16-Bit counters (C0~C199). The range of preset value is between 0~32767. C0~C139 are Retentive Counters and the CV value will be retained when the PLC turns on or RUN again after a power failure or a PLC STOP. For Non Retentive Counters, if a power failure or PLC STOP occurs, the CV value will be reset to 0 when the PLC turns on or RUN again.</div></div><div><div></div><div>There are total 56 32-Bit counters (C200~C255). The range of the preset value is between 0~2147483647. C200~C239 are Retentive Counters and C240~C255 are Non Retentive Counters.</div></div><div><div></div><div>The default number and assignment of the counters are shown below, if necessary can use the "CONFIGURATION" function to change the settings.</div></div><div><div></div><div>To insure the proper counting, the sustain time of input status of CLK should greater than 1 scan time.</div></div><div><div></div><div>The max. counting frequency with this instruction can only up to 20Hz, for higher frequency please use the high-speed soft/hardware counter.</div></div></div></div></div>																																																																			
Description	<div><div><div><div><div></div><div>When "CLR" is at 1, all of the contact Cn, FO0 (CUP), and CV value of the counter CV are cleared to 0 and the counter stops counting.</div></div><div><div></div><div>When "CLR" is at 0, the counter is allowed to count up. The Counter counts up every time the clock "CK ↑" changes from 0 to 1 (adds 1 to the CV) until the cumulative current value is equal to or greater than the preset value (CV>=PV), the counter "Count-Up" and the contact status of the counter Cn and FO0 (CUP) changes to 1. If the input status of clock continues to change, even the cumulative current value is equal and greater than the preset value, the CV value will still accumulate until it reaches the up limit at 32767 or 2147483647. The contact Cn and FO0 (CUP) stay at 1 as long as CV>=PV unless the "CLR" input is set to 1. (please refer the diagram ① below) ◦</div></div><div><div></div><div>If the FBs-PLC OS version is higher than V3.0 (inclusive), the M1973 can set to 1 so the CV will not accumulate further after "Count Up" and stops at the PV. M1973 default value is 0, therefore the status of M1973 can be set before executing any counter instruction in the program to individually set the counter CV to continue accumulating or stops at the PV after "Count Up" (please refer to the diagram ② below).</div></div></div></div></div>																																																																		

Basic Function Instruction

C	COUNTER (16-Bit: C0~C199, 32-bit: C200~C255)	C
Example 1	16-Bit Fixed Counter	
<div><div><div><div><div><div></div><div>RST</div><div>M1973</div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div>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C	COUNTER (16-Bit: C0~C199, 32-Bit: C200~C255)	C						
<table><tr><th>Ladder diagram</th><th>Key operations</th><th>Mnemonic code</th></tr><tr><td></td><td></td><td>ORG X 0 LD X 1 C200 PV: R 0 ORG C 200 OUT Y 1</td></tr></table>			Ladder diagram	Key operations	Mnemonic code			ORG X 0 LD X 1 C200 PV: R 0 ORG C 200 OUT Y 1
Ladder diagram	Key operations	Mnemonic code						
		ORG X 0 LD X 1 C200 PV: R 0 ORG C 200 OUT Y 1						
<p>Remark: If the preset value of the counter is 0 and "CLR" input also at 0, then the Cn contact status and F00 (CUP) becomes 1 immediately after the PLC finishes its first scan because the "Count-Up" has occurred. It will stay at 1 regardless how the CV value varies until "CLR" input changes to 1.</p>								

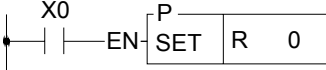

Basic Function Instruction

SET DP		SET (Set coil or all the bits of register to 1)		SET DP	
Symbol					
		Operand			
		Ladder symbol			
Set control — EN		<div><div>DP</div><div>SET</div><div>D</div></div>		D: destination to be set (the number of a coil or a register)	

SET DP	SET (Set coil or all the bits of register to 1)	SET DP
---------------	--	---------------

Example 2

Set 16-Bit Register

Ladder Diagram	Key Operations	Mnemonic Codes
		<div>ORGX0</div> <div>SETPR0</div>

B15 ↓

D	R0	1	0	1	1	0	1	1	0	1	1	1	0	1	1	0	0
---	----	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

B0 ↓

↓ X0 = ↑

B15 ↓

D	R0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
---	----	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

B0 ↓

[illegible]

Basic Function Instruction

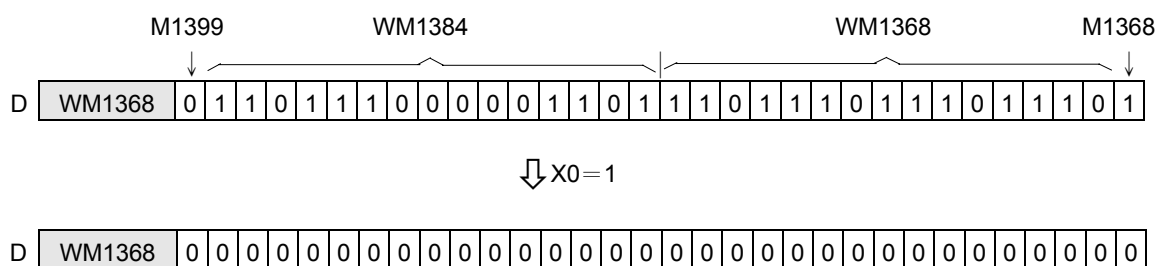
RST DP	RESET (Reset the coil or the register to 0)	RST DP																																																											
Symbol	<div><div><div>Ladder symbol</div><div><div>Reset control — EN</div><div><div>DP</div><div>RST</div><div>D</div></div></div></div><div><div>Operand</div><div>D: Destination to be reset (the number of a coil or a register)</div></div></div>																																																												
<table><tr><td>Range</td><td>Y</td><td>M</td><td>SM</td><td>S</td><td>WY</td><td>WM</td><td>WS</td><td>TMR</td><td>CTR</td><td>HR</td><td>OR</td><td>SR</td><td>ROR</td><td>DR</td></tr><tr><td rowspan="2">Ope- rand</td><td>Y0</td><td>M0</td><td>M1912</td><td>S0</td><td>WY0</td><td>WM0</td><td>WS0</td><td>T0</td><td>C0</td><td>R0</td><td>R3904</td><td>R3968</td><td>R5000</td><td>D0</td></tr><tr><td>Y255</td><td>M1911</td><td>M2001</td><td>S999</td><td>WY240</td><td>WM1896</td><td>WS984</td><td>T255</td><td>C255</td><td>R3839</td><td>R3967</td><td>R4167</td><td>R8071</td><td>D4095</td></tr><tr><td>D</td><td>○</td><td>○</td><td>○*</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○*</td><td>○*</td><td>○</td></tr></table>			Range	Y	M	SM	S	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	Ope- rand	Y0	M0	M1912	S0	WY0	WM0	WS0	T0	C0	R0	R3904	R3968	R5000	D0	Y255	M1911	M2001	S999	WY240	WM1896	WS984	T255	C255	R3839	R3967	R4167	R8071	D4095	D	○	○	○*	○	○	○	○	○	○	○	○	○*	○*	○
Range	Y	M	SM	S	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR																																															
Ope- rand	Y0	M0	M1912	S0	WY0	WM0	WS0	T0	C0	R0	R3904	R3968	R5000	D0																																															
	Y255	M1911	M2001	S999	WY240	WM1896	WS984	T255	C255	R3839	R3967	R4167	R8071	D4095																																															
D	○	○	○*	○	○	○	○	○	○	○	○	○*	○*	○																																															
Description	<div>● When the reset control "EN" =1 or from 0 → 1 (P instruction), resets the coil or register to 0.</div>																																																												
Example 1	Single Coil Reset																																																												
Please refer to example 1 for the SET instruction shown in page 6-8.																																																													
Example 2	16-Bit Register Reset																																																												
Ladder Diagram	Key Operations	Mnemonic Codes																																																											
<div><div>X0</div><div>— </div><div>— </div><div>—EN</div><div><div>P</div><div>RST</div><div>R 0</div></div></div>	<div><div>ORG</div><div>X^U</div><div>O[•]_{OPEN}</div><div>ENT</div><div>SET[•]_{RST}</div><div>SET[•]_{RST}</div><div>P^A</div><div>R^D</div><div>O[•]_{OPEN}</div><div>ENT</div></div>	<div>ORG X 0</div> <div>RST P R 0</div>																																																											

[illegible]

Example 3

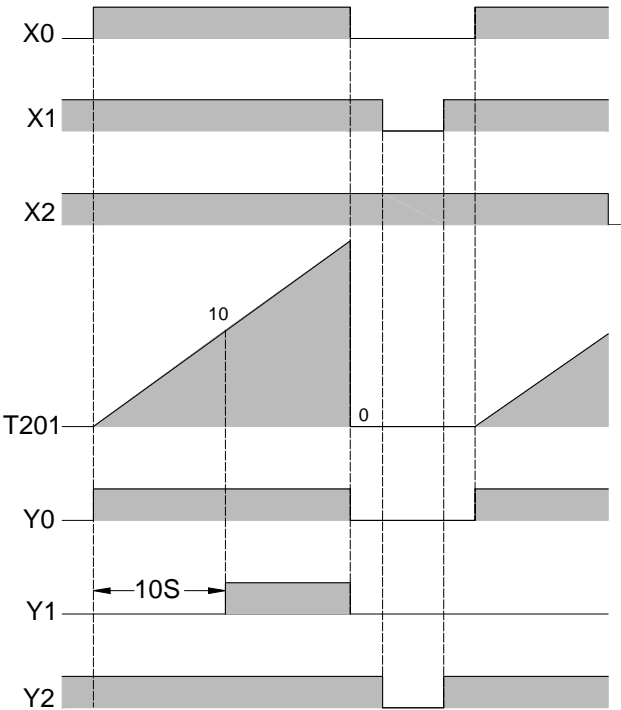
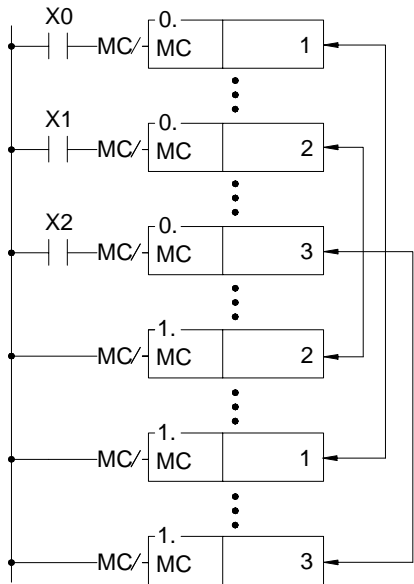
32-Bit Register Reset

Ladder Diagram	Key Operations	Mnemonic Codes
		<p>ORG X 0</p> <p>RST D WM1368</p>

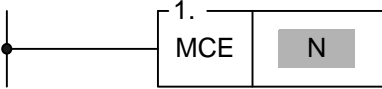


Basic Function Instruction

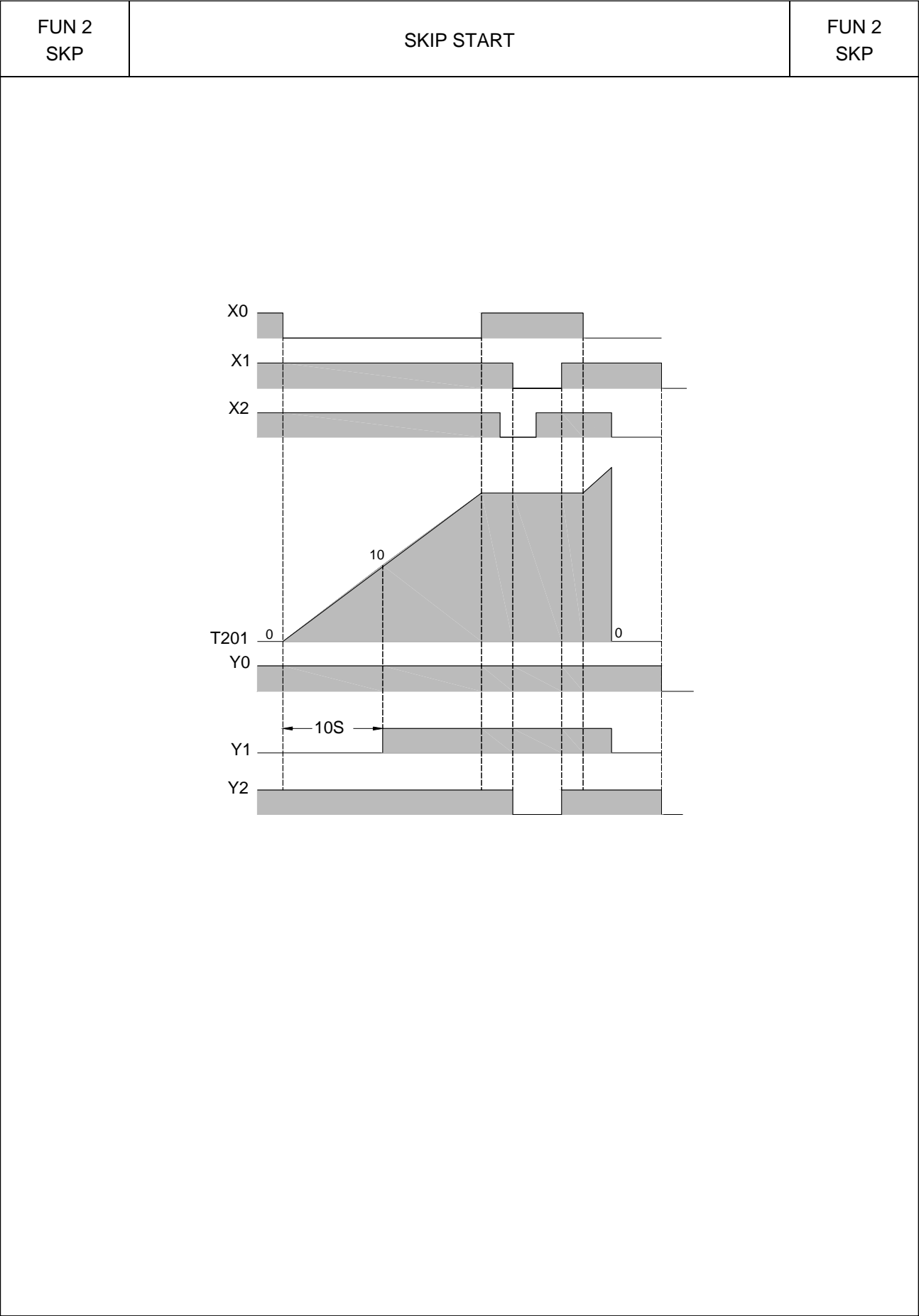
FUN 0 MC	MASTER CONTROL LOOP START	FUN 0 MC						
Symbol	<div><div><div>Ladder symbol</div><div>Master control — EN/—<div><div>0.<div>MC</div></div><div><div>N</div></div></div></div><div><div>Operand</div><div>N: Master Control Loop number (N=0~127) the number N cannot be used repeatedly.</div></div></div></div>							
Description	<div><div><div><div>●</div><div>There are a total of 128 MC loops (N=0~127). Every Master Control Start instruction, MC N, must correspond to a Master Control End instruction, MCE N, which has the same loop number as MC N. They must always be used in pairs and you should also make sure that the MCE N instruction is after the MC N instruction.</div></div><div><div>●</div><div>When the Master Control input "EN/" is 1, then this MC N instruction will not be executed, as it does not exist.</div></div><div><div>●</div><div>When the Master Control input "EN/" is 0, the master control loop is active, the area between the MC N and MCE N is called the Master Control active loop area. All the status of OUT coils or Timers within Master Control active loop area will be cleared to 0. Other instructions will not be executed.</div></div></div></div>							
Example	<table><tr><th>Ladder Diagram</th><th>Key Operations</th><th>Mnemonic Codes</th></tr><tr><td></td><td></td><td><div>ORGX0</div><div>FUN0</div><div>N:1</div><div>ORGX1</div><div>OUTY0</div><div>ORGX2</div><div>T201PV:10</div><div>ORG201</div><div>OUTY1</div><div>FUN1</div><div>N:1</div><div>ORGX1</div><div>OUTY2</div></td></tr></table>		Ladder Diagram	Key Operations	Mnemonic Codes			<div>ORGX0</div> <div>FUN0</div> <div>N:1</div> <div>ORGX1</div> <div>OUTY0</div> <div>ORGX2</div> <div>T201PV:10</div> <div>ORG201</div> <div>OUTY1</div> <div>FUN1</div> <div>N:1</div> <div>ORGX1</div> <div>OUTY2</div>
Ladder Diagram	Key Operations	Mnemonic Codes						
		<div>ORGX0</div> <div>FUN0</div> <div>N:1</div> <div>ORGX1</div> <div>OUTY0</div> <div>ORGX2</div> <div>T201PV:10</div> <div>ORG201</div> <div>OUTY1</div> <div>FUN1</div> <div>N:1</div> <div>ORGX1</div> <div>OUTY2</div>						

FUN 0 MC	MASTER CONTROL LOOP START	FUN 0 MC
<div></div> <div><p>Remark1:MC/MCE instructions can be used in nesting or interleaving as shown to the right:</p><p>Remark2: • When M1918=0 and the master input changes from 0→1, and if pulse type function instructions exist in the master control loop, then these instructions will have a chance to be executed only once (when the first time the master control input changes from 0→1). Afterwards, no matter how many times the master control input changes from 0→1, the pulse type function instructions will not be executed again.</p><ul style="list-style-type: none">• When M1918=1 and the master control input changes from 0→1, and if pulse type function instructions exist in the master control loop, then each time the master control input changes from 0→1 the pulse type function instructions in the master control loop will be executed as long as the action conditions are satisfied.• When a counting instruction exists in the master control loop, set M1918 to 0 can avoid counting error.• When the pulse type function instructions in the master control loop must act upon the 0→1 input change by the master control, the flag M1918 should be set to 1.</div> <div></div>		

Basic Function Instruction

FUN 1 MCE	MASTER CONTROL LOOP END	FUN 1 MCE
Symbol	<p><u>Operand</u></p> <p><u>Ladder symbol</u></p>  <p>N: Master Control End number (N=0~127) N can not be used repeatedly.</p>	
Description	<ul style="list-style-type: none"> ● Every MCE N must correspond to a Master Control Start instruction. They must always be used as a pair and you should also make sure that the MCE N instruction is after the MC N instruction. After the MC N instruction has been executed, all output coil status and timers will be cleared to 0 and no other instructions will be executed. The program execution will resume until a MCE instruction which has the same N number as MC N instruction appears. ● MCE instruction does not require an input control because the instruction itself forms a network which other instructions can not connect to it. If the MC instruction has been executed then the master control operation will be completed when the execution of the program reaches the MCE instruction. If MC N instruction has never been executed then the MCE instruction will do nothing. 	
Description	<ul style="list-style-type: none"> ● Please refer to the example and explanations for MC instruction. 	

FUN 2 SKP	SKIP START		FUN 2 SKP
Symbol	<div><div><div>Ladder symbol</div><div><div>Skip control — EN</div><div><div>2. SKP</div><div>N</div></div></div></div><div><div>Operand</div><div>N: Skip loop number (N=0~127), N can not be used repeatedly.</div></div></div>		
Description	<div><div><div><div>●</div><div>There are total 128 SKP loops (N=0~127). Every skip start instruction, SKP N, must correspond to a skip end instruction, SKPE N, which has the same loop number as SKP N. They must always be used as a pair and you should also make sure that the SKPE N instruction is after the SKP N instruction.</div></div><div><div>●</div><div>When the skip control "EN" is 0, then the Skip Start instruction will not be executed.</div></div><div><div>●</div><div>When the skip control "EN" is 1, the range between the SKP N and SKPE N which is so called the Skip active loop area will be skipped, that is all the instructions in this area will not be executed. Therefore the statuses of the discrete or registers in this Skip active loop area will be retained.</div></div></div></div>		
Example	<div><div><div><div>Ladder Diagram</div><div><div><div><div>X0</div><div>— </div><div>EN</div><div><div>2. SKP</div><div>1</div></div></div><div><div>X1</div><div>— </div><div></div><div><div>Y0</div><div>()</div></div></div><div><div>X2</div><div>— </div><div>EN</div><div><div>1S T201</div><div>10</div></div></div><div><div>T201</div><div>— </div><div></div><div><div>Y1</div><div>()</div></div></div><div><div></div><div>— </div><div></div><div><div>3. SKPE</div><div>1</div></div></div><div><div>X1</div><div>— </div><div></div><div><div>Y2</div><div>()</div></div></div></div></div><div><div>Key Operations</div><div><div><div>ORG</div><div>X^U</div><div>0[•] OPEN</div><div>ENT</div></div><div><div>FUN</div><div>2^F</div><div>ENT</div></div><div><div>1^E SHORT</div><div>ENT</div></div><div><div>ORG</div><div>X^U</div><div>1^E SHORT</div><div>ENT</div></div><div><div>OUT</div><div>Y^L</div><div>0[•] OPEN</div><div>ENT</div></div><div><div>ORG</div><div>X^U</div><div>2^F</div><div>ENT</div></div><div><div>T^V</div><div>2^F</div><div>0[•] OPEN</div><div>1^E SHORT</div><div>HEX</div></div><div><div>1^E SHORT</div><div>0[•] OPEN</div><div>ENT</div></div><div><div>ORG</div><div>T^V</div><div>2^F</div><div>0[•] OPEN</div><div>1^E SHORT</div><div>ENT</div></div><div><div>OUT</div><div>Y^L</div><div>1^E SHORT</div><div>ENT</div></div><div><div>FUN</div><div>3^G</div><div>ENT</div></div><div><div>1^E SHORT</div><div>ENT</div></div><div><div>ORG</div><div>X^U</div><div>1^E SHORT</div><div>ENT</div></div><div><div>OUT</div><div>Y^L</div><div>2^F</div><div>ENT</div></div></div></div><div><div>Mnemonic Codes</div><div><div>ORG</div><div>X</div><div>0</div></div><div><div>FUN</div><div>2</div></div><div><div>N :</div><div>1</div></div><div><div>ORG</div><div>X</div><div>1</div></div><div><div>OUT</div><div>Y</div><div>0</div></div><div><div>ORG</div><div>X</div><div>2</div></div><div><div>T201</div><div>PV :</div><div>10</div></div><div><div>ORG</div><div>T</div><div>201</div></div><div><div>OUT</div><div>Y</div><div>1</div></div><div><div>FUN</div><div>3</div></div><div><div>N :</div><div>1</div></div><div><div>ORG</div><div>X</div><div>1</div></div><div><div>OUT</div><div>Y</div><div>2</div></div></div></div></div></div>		



Basic Function Instruction

FUN 4 DIFU		DIFFERENTIAL UP				FUN 4 DIFU																
Symbol		<div><div><div><div><div>Ladder symbol</div><div><div>4.</div><div><div>Input status —TGU</div><div>DIFU</div></div><div><div>D</div></div></div></div><div><div>Operand</div><div>D: a specific coil number where the result of the Differential Up operation is stored.</div></div></div><div><table><tr><td>Range</td><td>Y</td><td>M</td><td>SM</td><td>S</td></tr><tr><td rowspan="2">Ope- rand</td><td>Y0 Y255</td><td>M0 M1911</td><td>M1912 M2001</td><td>S0 S999</td></tr><tr><td>D</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/>*</td><td><input type="radio"/></td></tr></table></div></div></div>						Range	Y	M	SM	S	Ope- rand	Y0 Y255	M0 M1911	M1912 M2001	S0 S999	D	<input type="radio"/>	<input type="radio"/>	<input type="radio"/> *	<input type="radio"/>
Range	Y	M	SM	S																		
Ope- rand	Y0 Y255	M0 M1911	M1912 M2001	S0 S999																		
	D	<input type="radio"/>	<input type="radio"/>	<input type="radio"/> *	<input type="radio"/>																	
Description		<div><div><div><div><div>●</div><div>The DIFU instruction is used to output the up differentiation of a node status (status input to "TGU") and the pulse signal resulting from the status change at the rising edge of the "TGU" for one scan time is stored to a coil specified by D.</div></div><div><div>●</div><div>The functionality of this instruction can also be achieved by using a TU contact.</div></div></div></div></div>																				
Example		The results of the following two samples are exactly the same																				
<div><div><div><div>Example 1</div><div><div><div>X1</div><div>TGU</div><div><div>4P.</div><div>DIFU</div><div>Y</div><div>0</div></div></div></div></div></div></div>		<div><div><div><div>ORG</div><div>X^U</div><div>1^E SHORT</div><div>ENT</div></div><div><div>FUN</div><div>4^I</div><div>ENT</div></div><div><div>Y^L</div><div>0^O OPEN</div><div>ENT</div></div></div></div>		<div><div><div>ORG</div><div>X</div><div>1</div></div><div><div>FUN</div><div>4</div></div><div><div>D :</div><div>Y</div><div>0</div></div></div>																		
<div><div><div><div>Example 2</div><div><div><div>X1</div><div>TU</div><div>Y0</div></div></div></div></div></div>		<div><div><div><div>ORG</div><div>TU^{<} TD</div><div>X^U</div><div>1^E SHORT</div><div>ENT</div></div><div><div>OUT</div><div>Y^L</div><div>0^O OPEN</div><div>ENT</div></div></div></div>		<div><div><div>ORG</div><div>TU</div><div>X</div><div>1</div></div><div><div>OUT</div><div>Y</div><div>0</div></div></div>																		

X1

Y0

t

t : scan time

FUN 5 P
DIFD

DIFFERENTIAL DOWN

FUN 5 P
DIFD

Symbol

Ladder symbol

Input status—TGD

5.
DIFD

D

Operand

N: a specific coil number where the result of the Differential Down operation is stored.

Range	Y	M	SM	S
Ope- rand	Y0	M0	M1912	S0
	Y255	M1911	M2001	S999
D	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>

Description

- The DIFD instruction is used to output the down differentiation of a node status (status input to "TGD") and the pulse signal resulting from the status change at the falling edge of the "TGD" for one scan time is stored to a coil specified by D.
- The functionality of this instruction can also be achieved by using a TD contact.

Example

The results of the following two samples are exactly the same

Ladder Diagram	Key Operations	Mnemonic Codes
<div>Example 1</div> <div></div>	<div></div>	<div>ORG X 1</div> <div>FUN 5</div> <div> D : Y 0</div>
<div>Example 2</div> <div></div>	<div></div>	<div>ORG TD X 1</div> <div>OUT Y 0</div>

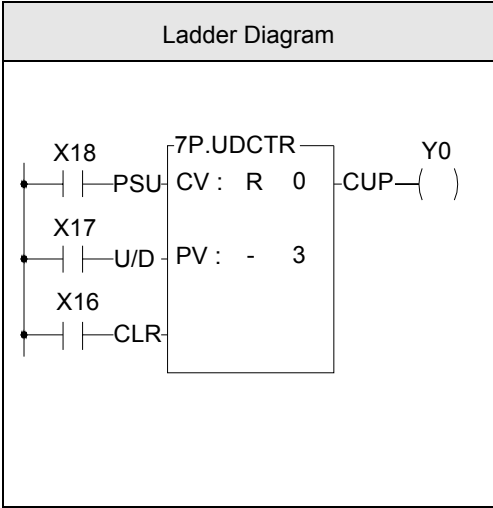
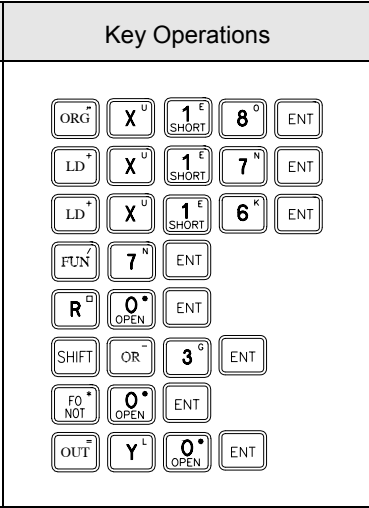
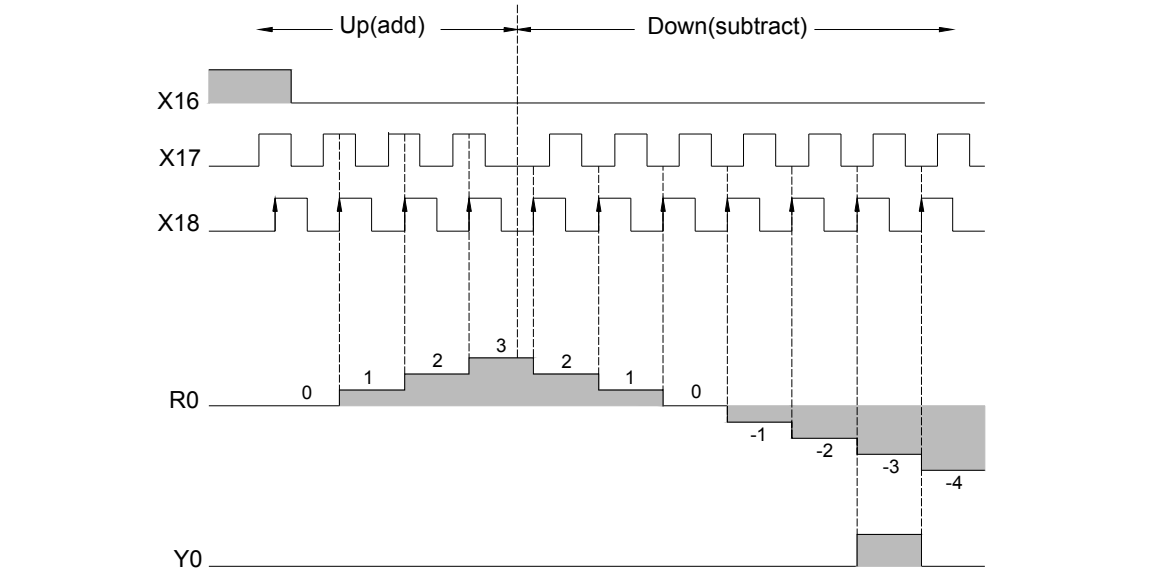
X1

Y0

t : scan time

6-19

FUN 7 DP UDCTR		UP/DOWN COUNTER (16-bit or 32-bit up and down 2-phase Counter)										FUN 7 DP UDCTR																																																																							
Symbol																																																																																			
		<div><div>Ladder symbol</div><div><div><div>7D.UDCTR</div><div>Clock — PLS — CV : <div></div></div><div>Up/Down count — U/D — PV : <div></div></div><div>Clear counter — CLR —</div></div><div>CUP — Count-UP (FO0)</div></div></div>										<div>Operand</div> <div>CV: The number of the Up/Down Counter PV: Preset value of the counter or it's register number</div>																																																																							
		<table><tr><td>Range</td><td>WX</td><td>WY</td><td>WM</td><td>WS</td><td>TMR</td><td>CTR</td><td>HR</td><td>IR</td><td>OR</td><td>SR</td><td>ROR</td><td>DR</td><td>K</td></tr><tr><td rowspan="2">Ope- rand</td><td>WX0</td><td>WY0</td><td>WM0</td><td>WS0</td><td>T0</td><td>C0</td><td>R0</td><td>R3840</td><td>R3904</td><td>R3968</td><td>R5000</td><td>D0</td><td rowspan="2">16/32-bit +/- number</td></tr><tr><td>WX240</td><td>WY240</td><td>WM1896</td><td>WS984</td><td>T255</td><td>C255</td><td>R3839</td><td>R3903</td><td>R3967</td><td>R4167</td><td>R8071</td><td>D4095</td></tr><tr><td>CV</td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td><td>○*</td><td>○*</td><td>○</td><td></td></tr><tr><td>PV</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td></tr></table>														Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	16/32-bit +/- number	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	CV		○	○	○	○	○	○		○	○*	○*	○		PV	○	○	○	○	○	○	○	○	○	○	○	○	○
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K																																																																						
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	16/32-bit +/- number																																																																						
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095																																																																							
CV		○	○	○	○	○	○		○	○*	○*	○																																																																							
PV	○	○	○	○	○	○	○	○	○	○	○	○	○																																																																						
Description		<div><div><div>●</div><div>When the clear control “CLR” is 1, the counter’s CV will be reset to 0 and the counter will not be able to count.</div></div><div><div>●</div><div>When the clear control “CLR” is 0, counting will then be allowed. The nature of the instruction is a P instruction. Therefore, when the count-pulse “PLS” is from 0→1 (rising edge), the CV will increased by 1 (if U/D=1) or decreased by 1 (if U/D=0).</div></div><div><div>●</div><div>When CV=PV, FO0(“Count-Up”) will change to 1”. If there are more clocks input, the counter will continue counting which cause CV≠PV. Then, FO0 will immediately change to 0. This means the “Count-Up” signal will only be equal to 1 if CV=PV, or else it will be equal to 0 (Care should be taken to this difference from the “Count-Up” signal of the general counter).</div></div><div><div>●</div><div>The upper limit of up count value is 32767 (16-bit) or 2147483647 (32-bit). After the upper limit is reached, if another up count clock is received, the counting value will become -32768 or -2147483648 (the lower limit of down count).</div></div><div><div>●</div><div>The lower limit of down count value is -32767 (16-bit) or -2147483647 (32-bit). After the lower limit is reached, if another down count clock is received, the counting value will become 32768 or 2147483648 (the upper limit of up count).</div></div><div><div>●</div><div>If U/D is fixed as 1, the instruction will become a single-phase up count counter. If U/D is fixed as 0, the instruction will become a single-phase down count counter.</div></div></div>																																																																																	

FUN 7 DP UDCTR	UP/DOWN COUNTER (16-bit or 32-bit up/down 2-phase Counter)	FUN 7 DP UDCTR																								
<div>Ladder Diagram</div> 	<div>Key Operations</div> 	<div>Mnemonic Codes</div> <table><tr><td>ORG</td><td>X</td><td>18</td></tr><tr><td>LD</td><td>X</td><td>17</td></tr><tr><td>LD</td><td>X</td><td>16</td></tr><tr><td>FUN</td><td>7</td><td></td></tr><tr><td></td><td>CV :</td><td>R 0</td></tr><tr><td></td><td>PV :</td><td>- 3</td></tr><tr><td>FO</td><td>0</td><td></td></tr><tr><td>OUT</td><td>Y</td><td>0</td></tr></table>	ORG	X	18	LD	X	17	LD	X	16	FUN	7			CV :	R 0		PV :	- 3	FO	0		OUT	Y	0
ORG	X	18																								
LD	X	17																								
LD	X	16																								
FUN	7																									
	CV :	R 0																								
	PV :	- 3																								
FO	0																									
OUT	Y	0																								
<div>Timing Diagram</div> 																										
<p>Remark 1: Since the counting operation of UDCTR is implemented by software scanning, therefore if the clock speed is faster than the scan speed, lose count may then happen (generally the clock should not exceed 20Hz depending on the size of the program). Please use the software or hardware high-speed counter in the PLC. Refer to the “High Speed Counter Application” in the Advanced Manual.</p>																										
<p>Remark 2: In order to ensure the proper counting, the sustain time of the status of clock input should greater than 1 scan time.</p>																										

FUN 8DP
MOV

MOVE
(Moves data from S to D)

FUN 8DP
MOV

Description

Ladder symbol

8DP.MOV

Move control — EN

S :

D :

Operand

S: Source register number
D: Destination register number
The S, N, D may combine with V, Z, P0~P9 to serve indirect addressing

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Operand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number	V · Z P0~P9
	S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>

Description

● Move (write) the data of S to a specified register D when the move control input "EN" =1 or from 0 to 1 (P instruction).

Example

Writes a constant data into a 16-bit register.

Ladder Diagram

X0

—|

—|

—EN

8P.MOV

S : 10

D : R 0

Key Operations

ORG

X^U

0[•]
OPEN

ENT

FUN

8⁰

P^A

ENT

1^E
SHORT

0[•]
OPEN

ENT

R^D

0[•]
OPEN

ENT

Mnemonic Codes

ORG

X

0

FUN

8P

S :

10

D :

R

0

S

K

10

⇓ X0 = ⌈

D

R0

10

6-23

Basic Function Instruction

FUN 9 D P MOV/		MOVE INVERSE (Inverts the data of S and moves the result to a specified device D)												FUN 9 D P MOV/																																																													
Symbol																																																																											
		<div><div>Ladder symbol</div><div><div>9DP.MOV/</div><div>Move control — EN</div><div>S : <div></div></div><div>D : <div></div></div></div></div>												<div><div>Operand</div><div>S: Source register number</div><div>D: Destination register number</div><div>S, N, D may combine with V, Z, P0~P9 to serve indirect addressing</div></div>																																																													
		<table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td rowspan="2">Ope- rand</td><td>WX0 WX240</td><td>WY0 WY240</td><td>WM0 WM1896</td><td>WS0 WS984</td><td>T0 T255</td><td>C0 C255</td><td>R0 R3839</td><td>R3840 R3847</td><td>R3904 R3967</td><td>R3968 R4167</td><td>R5000 R8071</td><td>D0 D4095</td><td>16/32-bit +/- number</td><td>V・Z P0~P9</td></tr><tr><td>S</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr><tr><td>D</td><td></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td><td><input checked="" type="radio"/></td><td><input checked="" type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td></tr></table>														Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3847	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number	V・Z P0~P9	S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input checked="" type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>		<input type="radio"/>
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Description		<div><div></div><div>Inverts the data of S (changes the status from 0 to 1 and from 1 to 0) and moves the results to a specified register D when the move control input "EN" =1 or from 0 to 1 (P instruction).</div></div>																																																																									
Example		Moves the inverted data of a 16-bit register to another 16-bit register.																																																																									
<div><div>Ladder Diagram</div><div><div><div>X0</div><div>•</div><div>— </div><div>— </div><div>EN</div></div><div><div>9.MOV/</div><div>S : R 0</div><div>D : WY 8</div></div></div></div>		<div><div>Key Operations</div><div><div><div>ORG</div><div>X</div><div>0</div><div>OPEN</div><div>ENT</div></div><div><div>FUN</div><div>9</div><div>ENT</div></div><div><div>R</div><div>0</div><div>OPEN</div><div>ENT</div></div><div><div>W</div><div>TR</div><div>Y</div><div>8</div><div>ENT</div></div></div></div>		<div><div>Mnemonic Codes</div><div><div>ORG</div><div>X</div><div>0</div><div>FUN</div><div>9</div><div>S :</div><div>R</div><div>0</div><div>D :</div><div>WY</div><div>8</div></div></div>																																																																							
		<div><div><div>S</div><div><div>R0</div><div><div>B15</div><div>0</div><div>1</div><div>0</div><div>1</div><div>0</div><div>1</div><div>0</div><div>1</div><div>0</div><div>1</div><div>0</div><div>1</div><div>0</div><div>1</div><div>B0</div></div></div><div>5555H</div></div><div><div>⇓ X0=1</div><div><div>D</div><div><div>WY8</div><div><div>Y23</div><div>1</div><div>0</div><div>1</div><div>0</div><div>1</div><div>0</div><div>1</div><div>0</div><div>1</div><div>0</div><div>1</div><div>0</div><div>1</div><div>0</div><div>Y8</div></div></div><div>AAAAH</div></div></div></div>																																																																									

FUN 10 TOGG	TOGGLE SWITCH (Changes the output status when the rising edge of control input occur)	FUN 10 TOGG																			
Symbol	<div><div><div>Ladder symbol</div><div>Input trigger —TGU—<div><div>10P. TOGG</div><div>D</div></div></div></div><div><div>Operand</div><div>D: the coil number of the toggle switch</div></div></div>																				
<table><tr><th>Range</th><th>Y</th><th>M</th><th>SM</th><th>S</th></tr><tr><td rowspan="2">Ope- rand</td><td>Y0 Y255</td><td>M0 M1911</td><td>M1912 M2001</td><td>S0 S999</td></tr><tr><td><input type="radio"/></td><td><input type="radio"/></td><td><input checked="" type="radio"/>*</td><td><input type="radio"/></td></tr><tr><td>D</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input checked="" type="radio"/></td><td><input type="radio"/></td></tr></table>			Range	Y	M	SM	S	Ope- rand	Y0 Y255	M0 M1911	M1912 M2001	S0 S999	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/> *	<input type="radio"/>	D	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>
Range	Y	M	SM	S																	
Ope- rand	Y0 Y255	M0 M1911	M1912 M2001	S0 S999																	
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D	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>																	
Description	<div><div></div><div>The coil D changes its status (from 1 to 0 and from 0 to 1) each time the input "TGU" is triggered from 0 to 1 (rising edge).</div></div>																				
Example	<table><tr><th>Ladder Diagram</th><th>Key Operations</th><th>Mnemonic Codes</th></tr><tr><td><div><div>X0</div><div>• TGU</div><div><div>10P. TOGG</div><div>Y 0</div></div></div></td><td><div><div>ORG</div><div>X^U</div><div>0^O OPEN</div><div>ENT</div><div>FUN</div><div>1^E SHORT</div><div>0^O OPEN</div><div>ENT</div><div>Y^L</div><div>0^O OPEN</div><div>ENT</div></div></td><td><div>ORG X 0</div><div>FUN 10</div><div><div>D :</div> Y 0</div></td></tr></table> <div><div>X0</div><div>Y0</div><div><div></div><div></div><div></div><div></div></div></div>		Ladder Diagram	Key Operations	Mnemonic Codes	<div><div>X0</div><div>• TGU</div><div><div>10P. TOGG</div><div>Y 0</div></div></div>	<div><div>ORG</div><div>X^U</div><div>0^O OPEN</div><div>ENT</div><div>FUN</div><div>1^E SHORT</div><div>0^O OPEN</div><div>ENT</div><div>Y^L</div><div>0^O OPEN</div><div>ENT</div></div>	<div>ORG X 0</div> <div>FUN 10</div> <div><div>D :</div> Y 0</div>													
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Basic Function Instruction

FUN 11 D P (+)		ADDITION (Performs addition of the data specified at Sa and Sb and stores the result in D)												FUN 11 D P (+)																																																																																																
Symbol																																																																																																														
Ladder symbol														Operand																																																																																																
<div><div>11DP.(+)</div><div><div>EN</div><div>Sa : <div></div></div><div>Sb : <div></div></div><div>U/S</div><div>D : <div></div></div><div>D=0 — Sum=0(FO0)</div><div>CY — Carry(FO1)</div><div>BR — Borrow(FO2)</div></div></div>														<div>Sa: Augend</div> <div>Sb: Addend</div> <div>D : Destination register to store the results of the addition</div> <div>Sa, Sb, D may combine with V, Z, P0~P9 to serve indirect addressing</div>																																																																																																
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Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																																																																																																
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																																																																																																
D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>																																																																																																
Description																																																																																																														
<div>● Performs the addition of the data specified at Sa and Sb and writes the results to a specified register D when the add control input "EN" =1 or from 0 to 1 (P instruction). If the result of addition is equal to 0 then set FO0 to 1. If carry occurs (the result exceeds 32767 or 2147483647) then set FO1 to 1. If borrow occurs (adding negative numbers resulting in a sum less than -32768 or -2147483648), then set the FO2 to 1. All the FO statuses are retained until this instruction is executed again and overwritten by a new result.</div>																																																																																																														
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<table><tr><td>Ladder Diagram</td><td>Key Operations</td><td>Mnemonic Codes</td></tr><tr><td><div><div>X0</div><div>EN</div><div>11P.(+)</div><div>Sa : R 0</div><div>Sb : R 1</div><div>U/S</div><div>D : R 2</div><div>D=0—</div><div>CY—()</div><div>BR—</div></div></td><td><div><div>ORG</div><div>X</div><div>0</div><div>ENT</div><div>FUN</div><div>1</div><div>1</div><div>P</div><div>ENT</div><div>R</div><div>0</div><div>ENT</div><div>R</div><div>1</div><div>ENT</div><div>R</div><div>2</div><div>ENT</div><div>FO</div><div>1</div><div>ENT</div><div>OUT</div><div>Y</div><div>0</div><div>ENT</div></div></td><td><div>ORG X 0</div><div>FUN 11P</div><div>Sa : R 0</div><div>Sb : R 1</div><div>D : R 2</div><div>FO 1</div><div>OUT Y 0</div></td></tr></table>														Ladder Diagram	Key Operations	Mnemonic Codes	<div><div>X0</div><div>EN</div><div>11P.(+)</div><div>Sa : R 0</div><div>Sb : R 1</div><div>U/S</div><div>D : R 2</div><div>D=0—</div><div>CY—()</div><div>BR—</div></div>	<div><div>ORG</div><div>X</div><div>0</div><div>ENT</div><div>FUN</div><div>1</div><div>1</div><div>P</div><div>ENT</div><div>R</div><div>0</div><div>ENT</div><div>R</div><div>1</div><div>ENT</div><div>R</div><div>2</div><div>ENT</div><div>FO</div><div>1</div><div>ENT</div><div>OUT</div><div>Y</div><div>0</div><div>ENT</div></div>	<div>ORG X 0</div> <div>FUN 11P</div> <div>Sa : R 0</div> <div>Sb : R 1</div> <div>D : R 2</div> <div>FO 1</div> <div>OUT Y 0</div>																																																																																											
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<table><tr><td>Sa</td><td>R0</td><td>12345</td><td rowspan="2">R0 + R1 = 32770</td></tr><tr><td>Sb</td><td>R1</td><td>20425</td></tr></table> <div>↕ X0 = ↕</div> <table><tr><td>D</td><td>R2</td><td>2</td><td>32768+2=32770</td></tr></table> <div>Y0=1 (carry 1 represents +32768)</div>														Sa	R0	12345	R0 + R1 = 32770	Sb	R1	20425	D	R2	2	32768+2=32770																																																																																						
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FUN 12 **DP**
(-)

SUBTRACTION
(Performs subtraction of the data specified at Sa and Sb and stores the result in D)

FUN 12 **DP**
(-)

Symbol

Ladder symbol

12DP.(-) —

Subtraction control — EN — Sa : — D=0 — Difference=0(FO0)

Unsign/Sign — U/S — Sb :

D : — CY — Carry(FO1)

— BR — Borrow(FO2)

Operand

Sa: Minuend

Sb: Subtrahend

D : Destination register to store the results of the subtraction

Sa, Sb, D may combine with V, Z, P0~P9 to serve indirect addressing

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number	V · Z P0~P9
	Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
D	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

Description

● Performs the subtraction of the data specified at Sa and Sb and writes the results to a specified register D when the subtract control input "EN" =1 or from 0 to 1 (**P** instruction). If the result of subtraction is equal to 0 then set FO0 to 1. If carry occurs (subtracting a negative number from a positive number and the result exceeds 32767 or 2147483647), then set FO1 to 1. If borrow occurs (subtracting a positive number from a negative number and the resulted difference is less than -32768 or -2147483648), then set FO2 to 1. All the FO statuses are retained until this instruction is executed again and overwritten by a new result.

Example

16-bit subtraction

Ladder Diagram

X0

—| |— EN

12P.(-) —

Sa : R 0 — D=0—

Sb : R 1 —

- U/S — D : R 2 — CY—

— BR — Y2 ()

Key Operations

ORG **X**^U **0**^{OPEN} ENT

FUN **1**^{SHORT} **2**^F ENT

R^D **0**^{OPEN} ENT

R^D **1**^{SHORT} ENT

R^D **2**^F ENT

FO^{*} **2**^F ENT

OUT **Y**^L **2**^F ENT

Mnemonic Codes

ORG X 0

FUN 12

Sa : R 0

Sb : R 1

D : R 2

FO 2

OUT Y 2

Sa R0 -5

Sb R1 32767

R0 - R1 = -32772

⇓ X0=1

D R2 -4

-32768 -4 = -32772

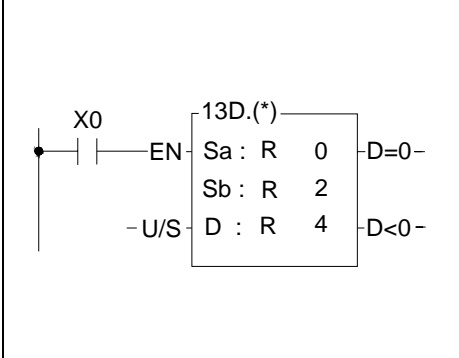
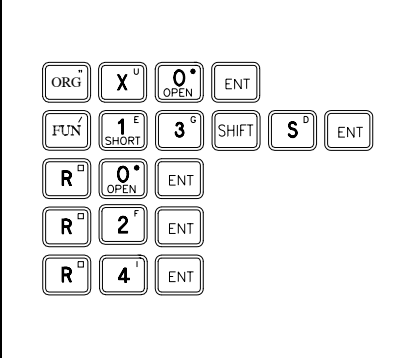
Y2=1 (borrow 1 represents -32768) Please refer to section 5.5

Basic Function Instruction

FUN 13 D P (*)		MULTIPLICATION (Performs multiplication of the data specified at Sa and Sb and stores the result in D)										FUN 13 D P (*)																																																																											
<div><div>Symbol</div><div><div><div><div><div>13DP.(*)</div><div>Multiplication control — EN</div><div>Sa : <div></div></div><div>Sb : <div></div></div><div>Unsign/Sign — U/S</div><div>D : <div></div></div></div><div><div>D=0 — Product=0(FO0)</div><div>D<0 — Product is negative (FO1)</div></div></div></div><div><div>Operand</div><div>Sa: Multiplicand Sb: Multiplier D : Destination register to store the results of the multiplication. Sa, Sb, D may combine with V, Z, P0~P9 to serve indirect addressing</div></div></div></div>																																																																																							
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<div><div>Description</div><div><div>●</div><div>Performs the multiplication of the data specified at Sa and Sb and writes the results to a specified register D when the multiplication control input "EN" =1 or from 0 to 1 (P instruction). If the product of multiplication is equal to 0 then set FO0 to 1. If the product is a negative number, then set FO1 to 1.</div></div></div>																																																																																							
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<div><div><div>Sa</div><div><div>R0</div><div>12345</div></div><div>Multiplicand</div></div><div>x</div><div><div>Sb</div><div><div>R1</div><div>4567</div></div><div>Multiplier</div></div><div><div>D</div><div><div>R3</div><div>R2</div><div>56379615</div></div><div>Product</div></div></div>																																																																																							

FUN 13 D P (*)	MULTIPLICATION (Performs multiplication of the data specified at Sa and Sb and stores the result in D)	FUN 13 D P (*)
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Example 2	32-bit multiplication
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Ladder Diagram	Key Operations	Mnemonic Codes
		ORG X 0 FUN 13D Sa : R 0 Sb : R 2 D : R 4

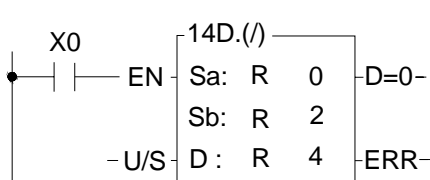
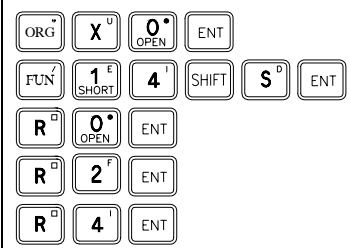
		R1		R0		Multiplicand			
Sa		12345678							
×	Sb	R3		R2		Multiplier			
<hr/>									
D	R7		R6		R5		R4		Product
	5629629168								

Basic Function Instruction

FUN 14 <div><div>D</div><div>P</div></div> <div>(/)</div>		DIVISION (Performs division of the data specified at Sa and Sb and stores the result in D)										FUN 14 <div><div>D</div><div>P</div></div> <div>(/)</div>																																																																																										
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<div><div><div>Ladder symbol</div><div><div>14DP.(/)</div><div><div>Division control — EN</div><div>Sa : <div></div></div><div>Sb : <div></div></div><div>Unsign/Sign — U/S</div><div>D : <div></div></div></div><div><div>D=0 — Quotient=0 (FO0)</div><div>ERR — Divisor is 0 (FO1)</div></div></div><div><div>Operand</div><div>Sa: Dividend</div><div>Sb: Divisor</div><div>D : Destination register to store the results of the division.</div><div>Sa, Sb, D may combine with V, Z, P0~P9 to serve indirect addressing</div></div></div></div>																																																																																																						
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Sa	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>																																																																																								
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D		<div></div>	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>		<div></div>	<div>*</div>	<div>*</div>	<div></div>		<div></div>																																																																																								
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<div><div></div><div>Performs the division of the data specified at Sa and Sb and writes the quotient and remainder to registers specified by register D when the division control input "EN" =1 or from 0 to 1 (<div>P</div> instruction). If the quotient of division is equal to 0 then set FO0 to 1. If the divisor Sb=0 then set the error flag FO1 to 1 without executing the instruction.</div></div>																																																																																																						
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FUN 14 D P (/)	DIVISION (Performs division of the data specified at Sa and Sb and stores the result in D)	FUN 14 D P (/)
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Example 2	32-bit division
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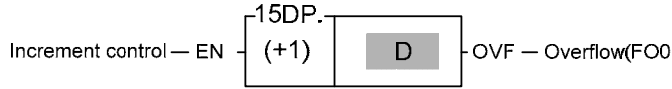
Ladder Diagram	Key Operations	Mnemonic Codes
		ORG X 0 FUN 14D Sa : R 0 Sb : R 2 D : R 4

Sa	R1	R0	Dividend
	2147483647		
Sb	R3	R2	Divisor
	1234567		
÷			
D	R7	R6	Remainder
	571634		
	R5	R4	Quotient
	1739		

Basic Function Instruction

FUN 15 D P (+1)	INCREMENT (Adds 1 to the D value)	FUN 15 D P (+1)
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Ladder symbol



Operand

D : The register to be increased
D may combine with V, Z, P0~P9 to serve indirect addressing

Range	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	XR
Ope- rand	WY0	WM0	WS0	T0	C0	R0	R3904	R3968	R5000	D0	V · Z
	WY240	WM1896	WS984	T255	C255	R3839	R3967	R4167	R8071	D4095	P0~P9
D	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

- Adds 1 to the register D when the increment control input "EN" =1 or from 0 to 1 (**P** instruction). If the value of D is already at the upper limit of positive number 32767 or 2147483647, adding one to this value will change it to the lower limit of negative number -32768 or -2147483648. At the same time, the overflow flag FO0 (OVF) is set to 1.

Example

16-bit increment register

Ladder diagram	Key operations	Mnemonic code
		<pre> ORG TU X 0 FUN 15 [D] : R 0V </pre>

When V = 100, 0 + 100 = 100

D **R100** 1

↓ X0 = ↑

D **R100** 2

FUN 16 D P (-1)	DECREMENT (Subtracts 1 from the D value)	FUN 16 D P (-1)
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Ladder symbol

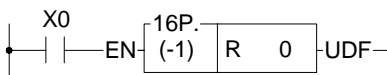
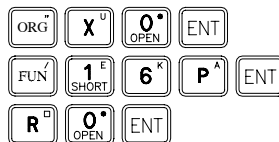
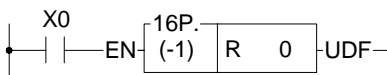
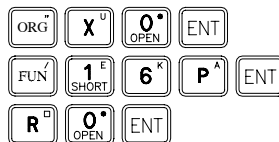
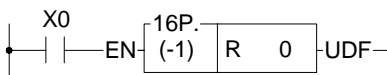
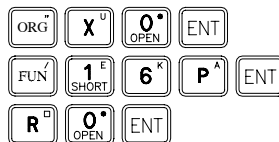
Operand



D : The register to be decreased
D may combine with V, Z, P0~P9 to serve indirect addressing

Range	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	XR
Ope- rand	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	V、Z P0~P9
	D	○	○	○	○	○	○	○*	○*	○	○

Description	<ul style="list-style-type: none">Subtracts 1 from the register D when the decrement control input "EN" =1 or from 0 to 1 (P instruction). If the value of D is already at the lower limit of negative number -32768 or -2147483648, subtracting one from this value will change it to the upper limit of positive number 32767 or 2147483647. At the same time, the underflow flag FO0 (UDF) is set to 1.
-------------	--

Example	16-bit decrement register							
<table><tr><th>Ladder diagram</th><th>Key operations</th><th>Mnemonic code</th></tr><tr><td></td><td></td><td><div>ORG X 0</div><div>FUN 16P</div><div><div>D :</div> R 0</div></td></tr></table>			Ladder diagram	Key operations	Mnemonic code			<div>ORG X 0</div> <div>FUN 16P</div> <div><div>D :</div> R 0</div>
Ladder diagram	Key operations	Mnemonic code						
		<div>ORG X 0</div> <div>FUN 16P</div> <div><div>D :</div> R 0</div>						
<div>D<div>R0<div>0</div></div></div> <div>⇩ X0=⇧</div> <div>D<div>R0<div>-1</div></div></div>								

Basic Function Instruction

FUN 17 D P CMP		COMPARE (Compares the data of Sa and Sb and outputs the results to function Outputs)												FUN 17 D P CMP																																																												
<div><div><div>Ladder symbol</div><div><div>17DP.CMP</div><div>Compare control — EN — Sa : <div></div></div><div>Unsign/Sign — U/S — Sb : <div></div></div></div><div><div>a = b — Sa=Sb (FO0)</div><div>a > b — Sa>Sb (FO1)</div><div>a < b — Sa<Sb (FO2)</div></div></div></div>														<div><div>Operand</div><div>Sa: The register to be compared</div><div>Sb: The register to be compared</div><div>Sa, Sb may combine with V, Z, P0~P9 to serve indirect addressing</div></div>																																																												
<table><tr><td>Range</td><td>WX</td><td>WY</td><td>WM</td><td>WS</td><td>TMR</td><td>CTR</td><td>HR</td><td>IR</td><td>OR</td><td>SR</td><td>ROR</td><td>DR</td><td>K</td><td>XR</td></tr><tr><td rowspan="2">Ope- rand</td><td>WX0 WX240</td><td>WY0 WY240</td><td>WM0 WM1896</td><td>WS0 WS984</td><td>T0 T255</td><td>C0 C255</td><td>R0 R3839</td><td>R3840 R3903</td><td>R3904 R3967</td><td>R3968 R4167</td><td>R5000 R8071</td><td>D0 D4095</td><td>16/32 bit +/-number</td><td>V · Z P0~P9</td></tr><tr><td>Sa</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr><tr><td>Sb</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr></table>																Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32 bit +/-number	V · Z P0~P9	Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR																																																												
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	Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																																																												
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																																																												
<div><div><div></div><div>Compares the data of Sa and Sb when the compare control input "EN" =1 or from 0 to 1 (P instruction). If the data of Sa is equal to Sb, then set FO0 to 1. If the data of Sa>Sb, then set FO1 to 1. If the data of Sa<Sb, then set FO2 to 1. If the data of Sa < Sb, then set the FO2 to 1.</div></div></div>																																																																										
Example		Compares the data of 16-bit register																																																																								
<div><div>Ladder diagram</div><div><div><div>X0</div><div>— — EN</div><div>— U/S</div></div><div><div>17.CMP</div><div>Sa : R 0</div><div>Sb : R 1</div></div><div><div>a=b —</div><div>a>b —</div><div>a<b — ()</div></div><div>Y0</div></div></div>		<div><div>Key operations</div><div><div><div>ORG</div><div>X^U</div><div>0^O OPEN</div><div>ENT</div></div><div><div>FUN</div><div>1^S SHORT</div><div>7^N</div><div>ENT</div></div><div><div>R^D</div><div>0^O OPEN</div><div>ENT</div></div><div><div>R^D</div><div>1^S SHORT</div><div>ENT</div></div><div><div>FO[*] NOT</div><div>2^F</div><div>ENT</div></div><div><div>OUT</div><div>Y^U</div><div>0^O OPEN</div><div>ENT</div></div></div></div>				<div><div>Mnemonic code</div><div><div>ORG</div><div>X</div><div>0</div></div><div><div>FUN</div><div>17</div></div><div><div>Sa :</div><div>R</div><div>0</div></div><div><div>Sb :</div><div>R</div><div>1</div></div><div><div>FO</div><div>2</div></div><div><div>OUT</div><div>Y</div><div>0</div></div></div>																																																																				
<div><div><div></div><div>From the above example, we first assume the data of R0 is 1 and R1 is 2, and then compare the data by executing the CMP instruction. The FO0 and FO1 are set to 0 and FO2 (a<b) is set to 1 since a<b.</div></div><div><div><div></div><div>If you want to have the compound results, such as ≥、≤、< > etc., please send =、< and > results to relay first and then combine the result from the relays.</div></div></div><div><div><div></div><div>M1919=0, when this command in not executed, FO0, FO1, FO2 will remain in the status at last execution.</div></div></div><div><div><div></div><div>M1919=1, when this command in not executed, FO0, FO1, FO2 are all cleared to 0.</div></div></div><div><div><div></div><div>Control M1919 properly to obtain memory-holding function for functional command output.</div></div></div></div>																																																																										

FUN 18 **D** **P**
AND

LOGICAL AND

FUN 18 **D** **P**
AND

Ladder symbol

18DP.AND

Operation control — EN

Sa :

Sb :

D :

D=0 — Result is 0 (FO0)

Operand

Sa: The register to be ANDed

Sb: The register to be ANDed

D : The register to store the result of AND

The Sa, Sb, D may combine with V, Z, P0~P9 to serve indirect addressing application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32 bit +/-number	V · Z P0~P9
	Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>

- Performs logical AND operation for the data of Sa and Sb when the operation control input "EN" =1 or from 0 to 1 (**P** instruction). This operation compares the corresponding bits of Sa and Sb (B0~B15 or B0~B31). The bit in the D is set to 1 if both of the corresponding bits data of Sa and Sb is 1. The bit in the D is set to 0 if one of the corresponding bits is 0.

Example	Operation of 16-bit logical AND
---------	---------------------------------

Ladder diagram	Key operations	Mnemonic code
<div><div>X0</div><div>— / — EN</div><div><div>18P.AND</div><div>Sa : R 0</div><div>Sb : R 1</div><div>D : R 2</div></div><div>D=0 —</div></div>	<div><div>ORG</div><div>X^U</div><div>0^{OPEN}</div><div>ENT</div></div> <div><div>FUN</div><div>1^{SHORT}</div><div>8^{OPEN}</div><div>P^A</div><div>ENT</div></div> <div><div>R^D</div><div>0^{OPEN}</div><div>ENT</div></div> <div><div>R^D</div><div>1^{SHORT}</div><div>ENT</div></div> <div><div>R^D</div><div>2^{OPEN}</div><div>ENT</div></div>	<div>ORG X 0</div> <div>FUN 18P</div> <div><div>Sa :</div> R 0</div> <div><div>Sb :</div> R 1</div> <div><div>D :</div> R 2</div>

	B15		B0															
	↓		↓															
Sa	R0	1	0	1	1	1	0	1	1	0	1	1	0	1	1	0	1	
Sb	R1	1	1	1	0	1	1	1	0	1	0	1	0	0	0	1	1	0

↕ x0 = ↗

	B15		B0														
	↓		↓														
D	R2	1	0	1	0	1	0	1	0	0	0	1	0	0	1	0	0

Basic Function Instruction

FUN 19 **D** **P**

OR

LOGICAL OR

FUN 19 **D** **P**

OR

Ladder symbol

19DP.OR

Operation control — EN

Sa :

Sb :

D :

D=0 — Result is 0 (FO0)

Sa: The register to be ORed

Sb: The register to be ORed

D : The register to store the result of OR

The Sa, Sb, D may combine with V, Z, P0~P9 to serve indirect addressing

Operand

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32 bit +/-number	V・Z P0~P9
	Sa													
Sb														
D														

- Performs logical OR operation for the data of Sa and Sb when the operation control input "EN" =1 or from 0 to 1 (**P** instruction). This operation compares the corresponding bits of Sa and Sb (B0~B15 or B0~B31). The bit in the D is set to 1 if one of the corresponding of Sa or Sb is 1. The bit in the D is set to 0 if both of the corresponding bits of Sa and Sb is 0.

Example

Operation of 16-bit logical OR

Ladder diagram

Key operations

ORG

X^U

0^{*}
OPEN

ENT

FUN

1^E
SHORT

9^O

ENT

R^D

0^{*}
OPEN

ENT

R^D

1^E
SHORT

ENT

R^D

2^F

ENT

Mnemonic code

ORG

X

0

FUN

19

Sa:

R

0

Sb:

R

1

D:

R

2

B15

↓

B0

↓

Sa

R0

1

0

1

1

1

0

1

1

0

1

1

0

1

1

0

1

Sb

R1

1

1

1

0

1

1

1

0

1

0

1

0

0

1

1

0

↓ X0=1

B15

↓

B0

↓

D

R2

1

1

1

1

1

1

1

1

1

1

0

1

1

1

1

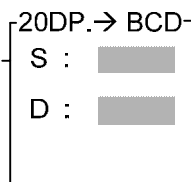
1

<p>FUN 20 D P →BCD</p>	<p>BIN TO BCD CONVERSION (Converts BIN data of the device specified at S into BCD and stores the result in D)</p>	<p>FUN 20 D P →BCD</p>
-----------------------------------	---	-----------------------------------

Ladder symbol

Operand

Conversion control — EN



- ERR — Error (FOO)

S : The register to be converted

D : The register to store the converted data
(BCD code)

The S, D may combine with V, Z, P0~P9 to serve indirect addressing

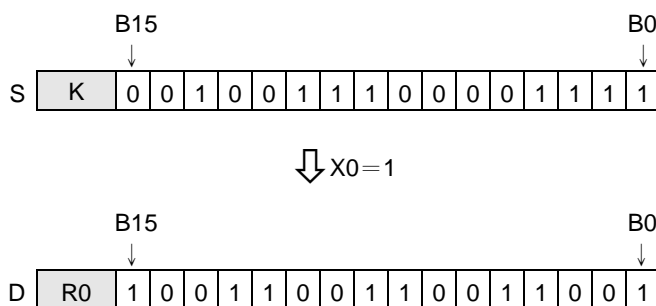
Range Oper- and	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3940 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32 bit +/- number	V · Z P0-P9
	S	○	○	○	○	○	○	○	○	○	○	○	○	○
D		○	○	○	○	○	○		○	○*	○*	○		○

- FB-PLC uses binary code to store and to execute calculations. If want to send the internal PLC data to the external displays such as seven-segment displays, it is more convenient for us to read the result on screen by converting the BIN data to BCD data. For example, it is more clear for us to read the reading "12" instead of the binary code "1100."
- Converts BIN data of the device specified at S into BCD and writes the result in D when the operation control input "EN" =1 or from 0 to 1 (**P** instruction). If the data in S is not a BCD value (0~9999 or 0~9999999), then the error flag FO0 is set to 1 and the old data of D are retained.

Example

16-bit BIN to BCD conversion

Ladder diagram	Key operations	Mnemonic code
		<p>ORG X 0</p> <p>FUN 20</p> <p>S : 9999</p> <p>D : R 0</p>



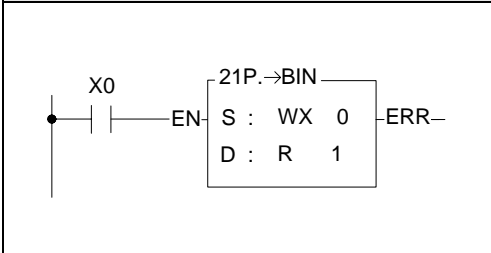
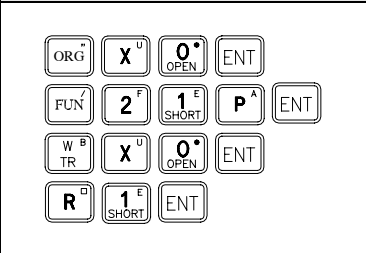
Basic Function Instruction

FUN 21 D P →BIN	BCD TO BIN CONVERSION (Converts BCD data of the device specified at S into BIN and stores the result in D)	FUN 21 D P →BIN
---	--	---

Ladder symbol		Operand	
Conversion control — EN	<div> <div>21DP.→BIN</div> <div> S : </div> <div> D : </div> </div>	ERR — Error (FO0)	S : The register to be converted D : The register to store the converted data (BIN code) The S, D may combine with V, Z, P0~P9 to serve indirect addressing

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	XR
Operand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	P0~P9
S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
D	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

- The decimal (BCD) data must be converted to binary (BIN) data first in order for PLC to accept the data which is originally in decimal unit (BCD code) inputted from external device such as digital switch because the BCD data can not be accepted by PLC for its operations.
- Converts BCD data of the device specified at S into BIN and writes the result in D when the operation control input "EN" =1 or from 0 to 1 (**P** instruction). If the data in S is not in BCD, then the error flag FO0 is set to 1 and the old data of D are retained.
- Constant is converted to BIN automatically when store in program and can not be used as a source operand of this function.

Example	16-bit BCD to BIN conversion																																			
<div>Ladder diagram</div> <div></div>	<div>Key operations</div> <div></div>	<div>Mnemonic code</div> <div><pre>ORG X 0 FUN 21P S : WX 0 D : R 1</pre></div>																																		
<div><div>X15</div><div>X0</div><div>S</div><div><table><tr><td>WX0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr></table></div><div>1</div><div>2</div><div>3</div><div>4</div></div> <div><div>↴ X0 = ↲</div></div> <div><div>B15</div><div>B0</div><div>D</div><div><table><tr><td>R1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr></table></div></div>			WX0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	R1	0	0	0	0	0	1	0	0	1	1	0	1	0	0	1	0
WX0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0																				
R1	0	0	0	0	0	1	0	0	1	1	0	1	0	0	1	0																				

Chapter 7 Advanced Function Instructions

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FUN22 P BREAK	BREAK FROM FOR AND NEXT LOOP (BREAK)	FUN22 P BREAK
<p style="text-align: center;"><u>Ladder symbol</u></p> <div><div>Execution control — EN</div><div><div>22P.</div><div>Break</div></div></div>		
<div><div><div><div>●</div><div>When execution control “EN” =1 or changes from 0→1 (P instruction) , it will terminate the FOR and NEXT program loop ◦</div></div><div><div>●</div><div>The program within the FOR and NEXT loop will be executed N times (N is assigned by FOR instruction) successively , but if it is necessary to terminate the execution loop less than N times , the BREAK instruction is necessary to apply ◦</div></div><div><div>●</div><div>The BREAK instruction must be located within the FOR and NEXT program loop ◦</div></div></div><div><div><div><div><div>EN</div><div>RST</div><div>V</div></div><div>70</div><div>FOR</div><div>D10</div><div>EN</div><div>17.CMP</div><div>Sa : D100</div><div>Sb : R0V</div><div>a=b ()</div><div>a>b —</div><div>a<b —</div><div>M200</div><div>M200</div><div>EN</div><div>BREAK</div><div>EN</div><div>15</div><div>(+1)</div><div>V</div><div>OVF—</div><div>71</div><div>NEXT</div><div>EN</div><div>08.MOV</div><div>S : V</div><div>D : D1000</div></div></div></div><div><div>Description : The loop count used to execute the FOR and NEXT program loop is assigned by register D10 ; the program within the FOR and NEXT loop is designed to search the same data storing in D100 from the register table starting at R0 ◦ If it finds , the searching loop will be terminated and then it goes to execute the program after the NEXT instruction ; If it doesn't find , the searching loop will be executed N times (N is the content of D10) and then it goes to execute the program after the NEXT instruction ◦ M200 tells the status and D100 is the pointer of searching ◦</div></div></div>		

FUN 23 P DIV48	48-BIT DIVISION	FUN 23 P DIV48
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FUN 24 D P SUM		SUM (Summation of block data)												FUN 24 D P SUM																																																																																										
Operation control — EN		<div>Ladder symbol</div> <div>24DP.SUM</div> <div>S : <div></div></div> <div>N : <div></div></div> <div>D : <div></div></div>														<div>S : Starting number of source register</div> <div>N : Number of registers to be summed (successive N data units starting from S)</div> <div>D : The register which stored the result (summation)</div> <div>S, N, D, can associate with V, Z, P0~P9 index register to serve the indirect addressing application.</div>																																																																																								
		<table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td rowspan="2">Ope- rand</td><td>WX0</td><td>WY0</td><td>WM0</td><td>WS0</td><td>T0</td><td>C0</td><td>R0</td><td>R3840</td><td>R3904</td><td>R3968</td><td>R5000</td><td>D0</td><td>1</td><td>V · Z</td></tr><tr><td>WX240</td><td>WY240</td><td>WM1896</td><td>WS984</td><td>T255</td><td>C255</td><td>R3839</td><td>R3903</td><td>R3967</td><td>R4167</td><td>R8071</td><td>D4095</td><td>511</td><td>P0~P9</td></tr><tr><td>S</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td></tr><tr><td>N</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr><tr><td>D</td><td></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td></tr></table>														Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	1	V · Z	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	511	P0~P9	S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	N	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>
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<div><div><div>● When operation control “EN”=1 or changes from 0→1 (P instruction), it puts the successive N units of 16bit or 32 bit (D instruction) registers for addition calculation to get the summation, and stores the result into the register which is designated by D.</div><div>● When the value of N is 0 or greater than 511, the operation will not be performed.</div><div>● Communication port1~4 can be used to serve as a general purpose ASCII communication interface. If the data error detecting method is Checksum, this instruction can be used to generate the sum value for sending data or ot use this instruction to check if the received data is error or not.</div></div><div><div>〈 Example 1 〉 When M1 changes from OFF→ON, following instruction will calculates the summation for 16-bit data.</div><div><div><div><div>M1</div><div>— EN</div></div><div><div>24P.SUM</div><div>S : R0</div><div>N : 6</div><div>D : R100</div></div></div><div><div><div>R0=0030H</div><div>R1=0031H</div><div>R2=0032H</div><div>R3=0033H</div><div>R4=0034H</div><div>R5=0035H</div></div><div>→ R100=012FH</div></div><div><div>● The left illustrates that 6 16-bit registers starting from R0 is calculated for summation, and the result is stored into the R100 register.</div></div></div><div><div>〈 Example 2 〉 When M1 is ON, it calculates the summation for 32-bit data.</div><div><div><div><div>M1</div><div>— EN</div></div><div><div>24D.SUM</div><div>S : R0</div><div>N : 3</div><div>D : R100</div></div></div><div><div><div>R1 , R0=00310030H</div><div>R3 , R2=00330032H</div><div>R5 , R4=00410039H</div></div><div>→ R101 , R100=00A5009BH</div></div><div><div>● The left illustrates that three 32-bit registers starting from DR0, is calculated for their summation, and the result is stored into the DR100 register.</div></div></div></div></div></div>																																																																																																								

FUN 25 D P MEAN	MEAN (Average of the block data)	FUN 25 D P MEAN
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Ladder symbol

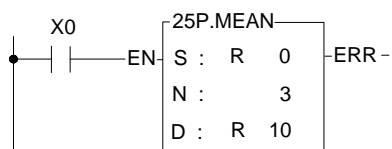
Operation control — EN — **25DP.MEAN** — ERR — N range error

S : N : D :

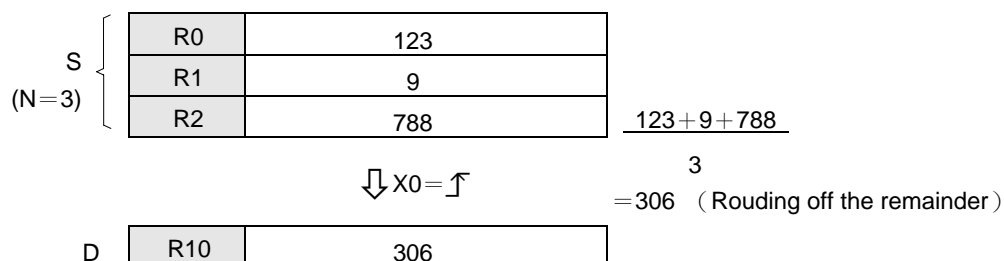
S : Source register number
N : Number of registers to be averaged (N units of successive registers starting from S)
D : Register number for storing result (mean value)
The S, N, D may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	2	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	256	P0~P9
S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
N	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
D	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

- When operation control "EN" = 1 or from 0 to 1 (**P** instruction), add the N successive 16-bit or 32-bit (**D** instruction) numerical values starting from S, and then divided by N. Store this mean value (rounding off numbers after the decimal point) in the register specified by D.
- While the N value is derived from the content of the register, if the N value is not between 2 and 256, then the N range error "ERR" will be set to 1, and do not execute the operation.



- At left, the example program gets the mean value of the 3 successive 16-bit registers starting from R0, and stores the results into the 16-bit register R10



FUN 26 D P SQRT	SQUARE ROOT	FUN 26 D P SQRT
----------------------------------	-------------	----------------------------------

Ladder symbol

Operation control — EN —

26DP.SQRT

S :

D :

— ERR — S range error

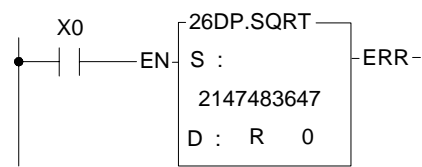
S : Source register to be taken square root

D : Register for storing result (square root value)

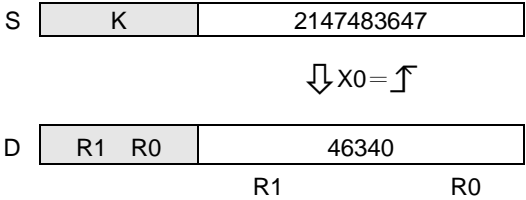
S, D may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit	V · Z P0~P9
S	○	○	○	○	○	○	○	○	○	○	○	○	○	○
D		○	○	○	○	○	○		○	○*	○*	○		○

- When operation control "EN" = 1 or from 0 to 1 (**P** instruction), take the square root (rounding off numbers after the decimal point) of the data specified by the S field, and store the result into the register specified by D.
- While the S value is derived from the content of the register, if the value is negative, then the S value error flag "ERR" will be set to 1, and do not execute the operation.



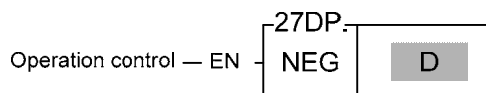
- The instruction at left calculates the square root of the constant 2147483647, and stores the result in R0.



$$\sqrt{2147483647} = 46340.\underline{95}$$

↑
rounding off

FUN 27 D P NEG	NEGATION (Take the negative value)	FUN 27 D P NEG
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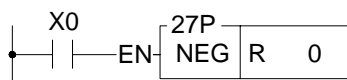
Ladder symbol

D : Register to be negated

D may combine with V, Z, P0~P9 to serve indirect address application

Range	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	XR
Ope- rand	WY0	WM0	WS0	T0	C0	R0	R3904	R3968	R5000	D0	V · Z
	WY240	WM1896	WS984	T255	C255	R3839	R3967	R4167	R8071	D4095	P0~P9
D	○	○	○	○	○	○	○	○*	○*	○	○

- When operation control "EN" = 1 or from 0 to 1 (**P** instruction), negate (ie. calculate 2's complement) the value of the content of the register specified by D, and store it back in the original D register.
- If the value of the content of D is negative, then the negation operation will make it positive.



- The instruction at left negates the value of the R0 register, and stores it back to R0.

D

R0	12345
----	-------

 ➞ 3039H

⇓ X0 = ⇑

D

R0	-12345
----	--------

 ➞ CFC7H

Arithmetical Operation Instructions

FUN 28 **D** **P**
ABS

ABSOLUTE
(Take the absolute value)

FUN 28 **D** **P**
ABS

Ladder symbol

Operation control — EN —

28DP.
ABS

D

D : Register to be taken absolute value
D may combine with V, Z, P0~P9 to serve indirect address application

Range	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	XR
Ope- rand	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	V · Z P0~P9
	D	○	○	○	○	○	○	○*	○*	○	○

- When operation control "EN" = 1 or from 0 to 1 (**P** instruction), calculate the absolute value of the content of the register specified by D, and write it back into the original D register.

X0

• — | — | — EN —

28DP.
ABS

R 0

- The instruction at left calculates the absolute value of the R0 register, and stores it back in R0.

D

R1	R0	-12345
----	----	--------

⇨ CFC7H

⇩ X0 = ⇧

D

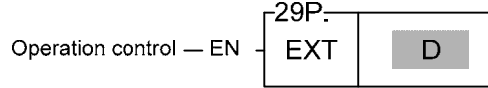
R1	R0	12345
----	----	-------

⇨ 3039H

7-7

FUN 29 D P EXT	SIGN EXTENSION	FUN 29 D P EXT
---------------------------------	----------------	---------------------------------

Ladder symbol

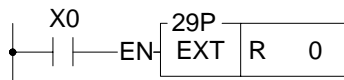


D : Register to be taken sign extension

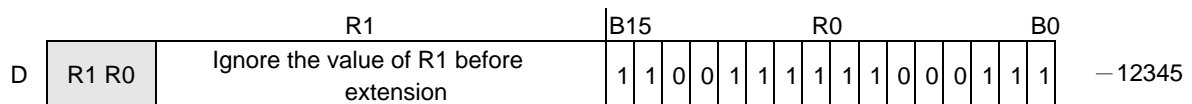
D may combine with V, Z, P0~P9 to serve indirect address application

Range	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	XR
Operand	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	V · Z P0~P9
D	○	○	○	○	○	○	○	○*	○*	○	○

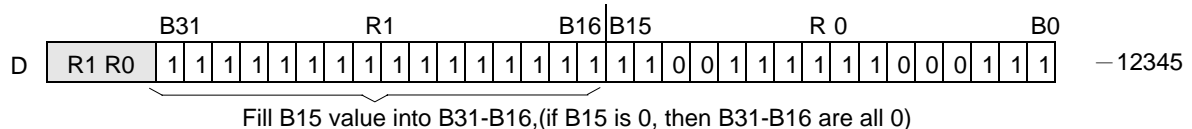
- When operation control "EN" = 1 or from 0 to 1 (**P** instruction), this instruction will sign extend the 16 bit numerical value specified by D to 32-bit value and store it into the 32-bit register comprised by the two successive words, D + 1 and D. (Both values are the same, only it was originally formatted as a 16 bit numerical value, and was then extended to be formatted as a 32 bit numerical value.)
- This instruction extent the numerical value of a 16-bit register into an equivalent numerical value in a 32-bit register (for example 33FFH converts to 000033FFH), Its main function is for numerical operations (+, -, *, /, CMP,.....) which can take the 16 bit or 32 bit numerical values as operand. Before operation all the operand should be adjusted to the same length for proper operation.



- The instruction at left takes a 16 bit numerical value R0, and extends it to an equivalent value in 32 bits, then stores it into a 32 bit register (DR0=R1R0) comprised R0 and R1



⇓ X0 = ⇓



Before extension (16 bits) R0= CFC7H= - 12345
 After extension (32 bits) R1R0=FFFFCFC7H= - 12345 } The two numerical values are actually the same

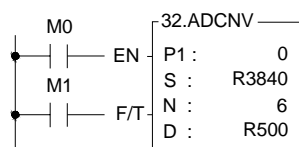
FUN 30 PID	GENERAL PURPOSE PID OPERATION (Brief description)				FUN 30 PID																																							
<div> <div> <div> <div> <div>Mode — A/M</div> <div>30.PID</div> <div>Ts : </div> </div> <div> <div>Bumpless — BUM</div> <div>SR : </div> <div>OR : </div> </div> <div> <div>Direction — D/R</div> <div>PR : </div> <div>WR : </div> </div> </div> <div> <div>ERR — Setting error</div> <div>HA — High alarm</div> <div>LA — Low alarm</div> </div> </div> </div> <div> <div> <div>Ts : PID Operation time interval</div> <div>SR : Starting register of process control parameter table comprised by 8 consecutive registers.</div> <div>OR : PID output register</div> <div>PR : Starting register of the process parameter table comprised by 7 consecutive registers.</div> <div>WR : Starting register of working variable for PID internal operation. It requires 7 registers and can't be re-used in other part of the ladder program.</div> </div> </div>																																												
<table> <tr> <th>Range</th> <th>HR</th> <th>ROR</th> <th>DR</th> <th>K</th> </tr> <tr> <td rowspan="2">Ope- rand</td> <td>R0</td> <td>R5000</td> <td>D0</td> <td></td> </tr> <tr> <td>R3839</td> <td>R8071</td> <td>D4095</td> <td></td> </tr> <tr> <td>Ts</td> <td><input type="radio"/></td> <td><input type="radio"/></td> <td><input type="radio"/></td> <td>1~3000</td> </tr> <tr> <td>SR</td> <td><input type="radio"/></td> <td><input type="radio"/></td> <td><input type="radio"/></td> <td></td> </tr> <tr> <td>OR</td> <td><input type="radio"/></td> <td><input type="radio"/></td> <td><input type="radio"/></td> <td></td> </tr> <tr> <td>PR</td> <td><input type="radio"/></td> <td><input type="radio"/></td> <td><input type="radio"/></td> <td></td> </tr> <tr> <td>WR</td> <td><input type="radio"/></td> <td><input type="radio"/></td> <td><input type="radio"/></td> <td></td> </tr> </table>						Range	HR	ROR	DR	K	Ope- rand	R0	R5000	D0		R3839	R8071	D4095		Ts	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	1~3000	SR	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		OR	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		PR	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		WR	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	
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WR	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																																									
<div> <div> <div> <div> <div>● PID function (FUN 30) according to the current value of process variable (PV) derived from the external analog signal and the Set Point (SP) of process performs the calculation, which base on the PID formula. The result of calculation is the control output for the controlled process, which can feed directly to the AO module or other output interface or leaved for further process. The usage of PID control for process if properly can achieve a fast and smooth result of PV tracking toward SP change or immune to the disturbance of process.</div> <div>● The PID formula in digital form:</div> </div> <div> $M_n = [(D4005/P_b) \times E_n] + \sum_0^n [(D4005/P_b) \times T_i \times T_s \times E_n] - [(D4005/P_b) \times T_d \times (P V_n - P V_{n-1}) / T_s] + \text{Bias}$ </div> <div> <div>M_n : Control output at time "n"</div> <div>D4005 : The gain constant, the default is 1000, which can be set between 1~5000.</div> <div>P_b : Proportional band (range : 2~5000, unit 0.1%. K_c (gain) =1000/ P_b)</div> <div>T_i : Intergral time constant (range : 0~9999 corresponds to 0.00~99.99 Repeats/Minute)</div> <div>T_d : Differential time constant (range : 0~9999 corresponds to 0.00~99.99 Minutes)</div> <div>PV_n : Process value at time "n"</div> <div>PV_{n-1} : Process value at time "n"</div> <div>E_n :Error at time "n" =set value (SP) – process value at time "n" (PV_n)</div> <div>T_s : Interval time of PID calculation (range: 1~3000, unit : 0.01 S)</div> <div>Bias : Control output offset (range: 0~16380)</div> </div> </div> </div> </div>																																												

FUN31 P CRC16	CRC16 CALCULATION (CRC16)	FUN31 P CRC16																																										
<div><div><div>Ladder symbol</div><div><div>31P.CRC16</div><div>MD : <div></div></div><div>S : <div></div></div><div>N : <div></div></div><div>D : <div></div></div></div><div>Execution control — EN</div></div><div><table><tr><th>Range</th><th>HR</th><th>ROR</th><th>DR</th><th>K</th></tr><tr><td></td><td>R0 R3839</td><td>R5000 R8071</td><td>D0 D4095</td><td></td></tr><tr><td>MD</td><td></td><td></td><td></td><td>0~1</td></tr><tr><td>S</td><td><div></div></td><td><div></div></td><td><div></div></td><td></td></tr><tr><td>N</td><td><div></div></td><td><div></div></td><td><div></div></td><td>1~256</td></tr><tr><td>D</td><td><div></div></td><td><div></div>*</td><td><div></div></td><td></td></tr></table></div></div> <div><div>MD : 0, Lower byte of registers to be calculated the CRC16</div><div>: 1, Reserved</div><div>S : Starting address of CRC16 calculation</div><div>N : Length of CRC16 calculation (In Byte)</div><div>D : The destination register to store the calculation of CRC16, Register D stores the Upper Byte of CRC16 Register D + 1 stores the Lower Byte of CRC16</div><div>S, N, D may associate with V · Z · P0~P9 index register to serve the indirect addressing application</div></div>			Range	HR	ROR	DR	K		R0 R3839	R5000 R8071	D0 D4095		MD				0~1	S	<div></div>	<div></div>	<div></div>		N	<div></div>	<div></div>	<div></div>	1~256	D	<div></div>	<div></div> *	<div></div>													
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D	<div></div>	<div></div> *	<div></div>																																									
<div><div><div><div>When execution control "EN"=1 or changes from 0→1 (P instruction, it will start the CRC16 calculation from the lower byte of S and by the length of N, the result of calculation will be stored into register D and D+1.</div><div>The output indication "D=0" will be ON if the value of calculation is 0.</div><div>It will not execute the calculation and the output indication "ERR" will be ON if the length is invalid.</div><div>When communicating with the intelligent peripheral in binary data format, the CRC16 error detection is used very often; the well known Modbus RTU communication protocol uses this method for error detection of message frame.</div><div>CRC16 is the check value of a Cyclical Redundancy Check calculation performed on the message contents.</div><div>Perform the CRC16 calculation on the received message data and error check value, the result of the calculation value must be 0, it means no error within this message frame.</div></div></div></div> <div><div><div><div>M0</div><div><div>08P.MOV</div><div>S : D0</div><div>D : V</div></div></div><div><div>31P.CRC16</div><div>MD: 0</div><div>S : R0</div><div>N : D0</div><div>D : R0V</div><div>D=0 —</div><div>ERR —</div></div></div></div> <div><div>Description : When M0 changes from 0→1, it will execute the CRC16 calculation starting from lower byte of R0, the length is assigned by D0, and then stores the CRC value into register R0+V and R0+V+1.</div><div>It is supposed D0=10, the registers R10 and R11 will store the CRC16 value.</div></div> <div><div><div>S</div><div><table><tr><th></th><th>High Byte</th><th>Low Byte</th></tr><tr><td>R0</td><td>Don't care</td><td>Byte-0</td></tr><tr><td>R1</td><td>Don't care</td><td>Byte-1</td></tr><tr><td>R2</td><td>Don't care</td><td>Byte-2</td></tr><tr><td>R3</td><td>Don't care</td><td>Byte-3</td></tr><tr><td>R4</td><td>Don't care</td><td>Byte-4</td></tr><tr><td>R5</td><td>Don't care</td><td>Byte-5</td></tr><tr><td>R6</td><td>Don't care</td><td>Byte-6</td></tr><tr><td>R7</td><td>Don't care</td><td>Byte-7</td></tr><tr><td>R8</td><td>Don't care</td><td>Byte-8</td></tr><tr><td>R9</td><td>Don't care</td><td>Byte-9</td></tr></table></div></div><div><div>D</div><div><table><tr><th></th><th>High Byte</th><th>Low Byte</th></tr><tr><td>R10</td><td>00</td><td>CRC-Hi</td></tr><tr><td>R11</td><td>00</td><td>CRC-Lo</td></tr></table></div></div></div>				High Byte	Low Byte	R0	Don't care	Byte-0	R1	Don't care	Byte-1	R2	Don't care	Byte-2	R3	Don't care	Byte-3	R4	Don't care	Byte-4	R5	Don't care	Byte-5	R6	Don't care	Byte-6	R7	Don't care	Byte-7	R8	Don't care	Byte-8	R9	Don't care	Byte-9		High Byte	Low Byte	R10	00	CRC-Hi	R11	00	CRC-Lo
	High Byte	Low Byte																																										
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R11	00	CRC-Lo																																										

FUN32 ADCNV	CONVERTING THE RAW VALUE OF 4~20MA ANALOG INPUT (ADCNV)					FUN32 ADCNV
<div><div><div><div><div></div><div></div></div><div><div></div><div></div></div></div><div><div></div><div></div></div><div><div></div><div></div></div></div><div><div></div><div></div></div><div><div></div><div></div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> <div><div></div><div></div></div> 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FUN32 ADCNV	CONVERTING THE RAW VALUE OF 4~20mA ANALOG INPUT (ADCNV)	FUN32 ADCNV
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Example :



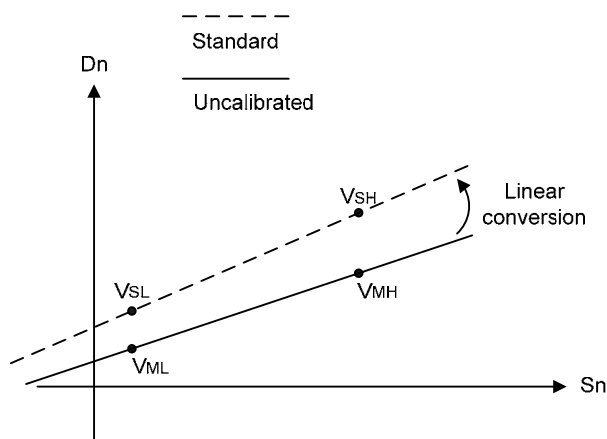
Description : When M0 is ON and M1 is OFF, it will perform 6 points of conversion starting from R3840, where the offset of 4~20mA raw reading value will be eliminated, and the corresponding value 0~4095 will be stored into R500~R505.

S		D		
R3840	−1229	R500	0	(4 mA)
R3841	409	R501	2047	(12 mA)
R3842	2047	R502	4095	(20 mA)
R3843	−2048	R503	0	(0 mA)
R3844	−2048	R504	0	(0 mA)
R3845	−2048	R505	0	(0 mA)

When M0 is ON and M1 is ON, it will perform 6 points of conversion starting from R3840, where the offset of 4~20mA raw reading value will be eliminated, and the corresponding value 0~16383 will be stored into R500~R505.

S		D		
R3840	−4916	R500	0	(4 mA)
R3841	1637	R501	8191	(12 mA)
R3842	8191	R502	16383	(20 mA)
R3843	−8192	R503	0	(0 mA)
R3844	−8192	R504	0	(0 mA)
R3845	−8192	R505	0	(0 mA)

FUN33 P LCNV	Linear Conversion (LCNV)	FUN33 P LCNV																																									
<div><div><div>Ladder symbol</div><div>33P.LCNV</div><div>Operation control — EN —</div><div>Md : <div></div></div><div>S : <div></div></div><div>Ts : <div></div></div><div>D : <div></div></div><div>L : <div></div></div></div><div><div>Md : Operation mode , 0~3</div><div>S : Starting address of the source data</div><div>Ts : Starting address of the parameter table for conversion</div><div>D : Starting address to store the result</div><div>L : Quantity of conversion entry , 1~64</div></div><table><tr><th rowspan="2">Operand \ Range</th><th>HR</th><th>IR</th><th>ROR</th><th>DR</th><th>K</th></tr><tr><td>R0 R3839</td><td>R3840 R3903</td><td>R5000 R8071</td><td>D0 D3999</td><td></td></tr><tr><td>Md</td><td></td><td></td><td></td><td></td><td>0~3</td></tr><tr><td>S</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td></tr><tr><td>Ts</td><td>○</td><td></td><td>○</td><td>○</td><td></td></tr><tr><td>D</td><td>○</td><td></td><td>○*</td><td>○</td><td></td></tr><tr><td>L</td><td>○</td><td></td><td>○</td><td>○</td><td>1~64</td></tr></table></div>			Operand \ Range	HR	IR	ROR	DR	K	R0 R3839	R3840 R3903	R5000 R8071	D0 D3999		Md					0~3	S	○	○	○	○		Ts	○		○	○		D	○		○*	○		L	○		○	○	1~64
Operand \ Range	HR	IR		ROR	DR	K																																					
	R0 R3839	R3840 R3903	R5000 R8071	D0 D3999																																							
Md					0~3																																						
S	○	○	○	○																																							
Ts	○		○	○																																							
D	○		○*	○																																							
L	○		○	○	1~64																																						
<div><div><div><div>● When the analog input module being used for the analog measurement, the raw reading value of the analog input can be converted into the engineering range through this instruction for display or for proceeding control operation.</div><div>● For process measurement calibration, making the linear conversion for the engineering process variable, which the measurement value from the PLC's can be corrected by the value from the standard meter's through this instruction.</div><div>● When execution control "EN"=1 or from 0→1(P instruction), this instruction will perform the linear conversion operation according to the mode selection, where S is the starting address of the source data, Ts is the starting address of the conversion parameter table, D is the starting address to store the converted result, and L is the quantity of conversion entry.</div><div>● There are two expressions to meet the suitable application:</div></div><div><div>Expression 1 : Two points calibration method</div><div><div>Fill the conversion parameter table with the low value of measurement(VML), high value of measurement(VMH), and the corresponding low value of standard (VSL), high value of standard(VSH); the converted result(Dn) will be generated from the source data(Sn) through the formula shown below:</div><div><div>A = (VSL - VSH / VML - VMH) × 10000</div><div>B = VSL - (VML × A / 10000)</div><div>Dn = (Sn × A / 10000) + B</div></div><div><div><div>• The range of operands VSL, VSH, VML, VMH, Sn and Dn are between -32768 ~ 32767</div><div>• For analog input scaling, where VML=Minum of analog input VMH=Maximum of analog input VSL=Minum of engineering range VSH=Maximum of engineering range</div></div></div></div><div><div><div><div><div><div></div><div>Dn</div></div><div><div></div><div>Standard</div></div><div><div></div><div>Uncalibrated</div></div></div><div><div><div><div>VSL</div><div>VMH</div><div>VML</div><div>VSH</div></div><div><div></div><div>Linear conversion</div></div></div><div><div></div><div>Sn</div></div></div></div></div></div></div></div></div>																																											



FUN33 P
LCNVLinear Conversion
(LCNV)FUN33 P
LCNV**Expression 2 : Multiplier + Offset method**

Fill the conversion parameter table with the values of multiplier(A), divisor(B) and offset(C);
The converted result(Dn) will be generated from the source data(Sn) through the formula shown below:

$$Dn = [(Sn \times A) / B] + C$$

The range of each operand as below:

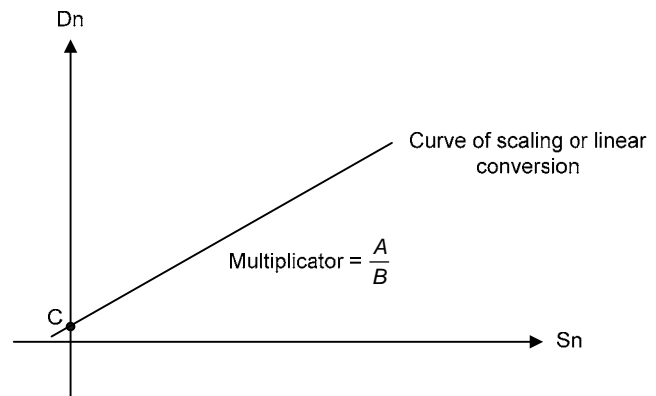
$$A = 1 \sim 65535$$

$$B = 1 \sim 65535$$

$$C = -32768 \sim 32767$$

$$Sn = 0 \sim 65535$$

$$Dn = -32768 \sim 32767$$

**Description of operation mode :**

1. When Md = 0, the linear conversion works by expression 1, and all source data share the same parameters VML · VMH · VSL and VSH for conversion.
2. When Md = 1, the linear conversion works by expression 1, and each source data has the independent corresponding parameters VML · VMH · VSL · VSH for conversion; if there are N entries of source data, the conversion parameter table should have N groups of VML · VMH · VSL · VSH for working, there are N×4 registers in the conversion parameter table.
3. When Md = 2, the linear conversion works by expression 2, and all source data share the same parameters A · B and C for conversion.
4. When Md = 3, the linear conversion works by expression 2, and each source data has the independent corresponding parameters A · B · C for conversion; if there are N entries of source data, the conversion parameter table should have N groups of A · B · C for working, there are N×3 registers in the conversion parameter table.

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Linear Conversion
(LCNV)

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Example program 1 : Mode 0 of linear conversion

N000

M0

EN

33.LCNV

Md: 0

S : R100

Ts: R1000

D : R2000

L : 6

Description : When M0 = 1, it will perform the mode 0 operation of linear conversion, where R100 is the starting address of the source data, R1000 is the starting address of the table of the conversion parameters VML、VMH、VSL、VSH, the quantity is 6, and R2000~R2005 will store the converted results.

Ts

R1000282

R10013530

R1002260

R10033650

VML

VMH

VSL

VSH

S

R100282

R1013530

R1021906

R1030

R1045000

R105-115

D

R2000260

R20013650

R20021955



R2003-34

R20045184

R2005-154

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LCNVLinear Conversion
(LCNV)FUN33 
LCNV

Example program 2 : Mode 1 of linear conversion



Description : When M0 = 1, it will perform the mode 1 operation of linear conversion, where R100 is the starting address of the source data, R1000 is the starting address of the table of the conversion parameters VML、VMH、VSL、VSH, the quantity is 3, and R2000~R2002 will store the converted results.

Ts

R1000	282	VML_0
R1001	3530	VMH_0
R1002	260	VSL_0
R1003	3650	VSH_0
R1004	-52	VML_1
R1005	1208	VMH_1
R1006	-38	VSL_1
R1007	1101	VSH_1
R1008	235	VML_2
R1009	4563	VMH_2
R1010	264	VSL_2
R1011	4588	VSH_2

S

R100	282
R101	1208
R102	2399



D

R2000	260
R2001	1101
R2002	2426

FUN33 P
LCNV

Linear Conversion
(LCNV)

FUN33 P
LCNV

Example program 3 : Mode 2 of linear conversion

N000

M0

EN

33.LCNV

Md: 2

S : R100

Ts: R1000

D : R2000

L : 6

Description : When M0 = 1, it will perform the mode 2 operation of linear conversion, where R100 is the starting address of the source data, R1000 is the starting address of the table of the conversion parameters A、B、C, the quantity is 6, and R2000~R2005 will store the converted results.

Ts

R1000985A

R10011000B

R100220C

S

R1001000

R1012345

R1023560

R103401

R104568

R1052680

D

R20001005

R20012330

R20023527

R2003415

R2004579

R20052660

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FUN33 P
LCNVLinear Conversion
(LCNV)FUN33 P
LCNV

Example program 4 : Mode 3 of linear conversion





Description : When M0 = 1, it will perform the mode 3 operation of linear conversion, where R100 is the starting address of the source data, R1000 is the starting address of the table of the conversion parameters A、B、C, the quantity is 4, and R2000~R2003 will store the converted results.

	Ts
R1000	5000
R1001	16380
R1002	0
R1003	10000
R1004	16383
R1005	0
R1006	2200
R1007	16380
R1008	-200
R1009	1600
R1010	16383
R1011	-100


	S		D
R100	8192	⇒	R2000 2501
R101	16383		R2001 10000
R102	8190		R2002 900
R103	0		R2003 -100

Multiple Linear Conversion

FUN34  MLC		Multiple Linear Conversion (MLC)					FUN34  MLC																																															
Execution Control EN		<div><div>34P. MLC</div><div><div>Rs :</div><div>SI :</div><div>Tx :</div><div>Ty :</div><div>TI :</div><div>D :</div></div><div>OVR</div></div>					<div><div>Rs : Starting address of the source data</div><div>SI : Quantity of source data, 1~64</div><div>Tx : Starting address of X table</div><div>Ty : Starting address of Y table</div><div>TI : Quantity of table, 2~255</div><div>D : Starting address to store the result</div></div>																																															
Selection X/Y		<table><tr><th>Range Operand</th><th>HR</th><th>IR</th><th>ROR</th><th>DR</th><th>K</th></tr><tr><td></td><td>R0 R3839</td><td>R3840 R3903</td><td>R5000 R8071</td><td>D0 D3999</td><td></td></tr><tr><td>Rs</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td></tr><tr><td>SI</td><td><input type="radio"/></td><td></td><td><input type="radio"/></td><td><input type="radio"/></td><td>1~64</td></tr><tr><td>Tx</td><td><input type="radio"/></td><td></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td></tr><tr><td>Ty</td><td><input type="radio"/></td><td></td><td><input checked="" type="radio"/></td><td><input type="radio"/></td><td></td></tr><tr><td>TI</td><td><input type="radio"/></td><td></td><td><input type="radio"/></td><td><input type="radio"/></td><td>2~255</td></tr><tr><td>D</td><td><input type="radio"/></td><td></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td></tr></table>					Range Operand	HR	IR	ROR	DR	K		R0 R3839	R3840 R3903	R5000 R8071	D0 D3999		Rs	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		SI	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	1~64	Tx	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>		Ty	<input type="radio"/>		<input checked="" type="radio"/>	<input type="radio"/>		TI	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	2~255	D	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	
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Tx	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>																																																		
Ty	<input type="radio"/>		<input checked="" type="radio"/>	<input type="radio"/>																																																		
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D	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>																																																		

When the analog input module being used for the analog measurement, the raw reading value of the analog input can be converted into the engineering range through this instruction for display or for proceeding control operation.

For process measurement calibration, making the linear conversion for the engineering process variable, which the measurement value from the PLC's can be corrected by the value from the standard meter's through this instruction.

When execution control "EN"=1 or from 0→1( instruction), this instruction will perform the multiple linear conversion operation according to the selection of X/Y input; where Rs is the starting address of the source data, SI is the quantity of source data for conversion, Tx is the starting address of X conversion parameter table, Ty is the starting address of Y conversion parameter table, TI is the quantity of X/Y table, D is the starting address to store the converted result.

When executing and selection X/Y=0, it will compare the source data with the entities of Tx table to find the corresponding location in Tx table (The entities in Tx table must be in ascending sequence), and then calculate the linear conversion according to the located section of Tx and Ty table;
When executing and selection X/Y=1, it will compare the source data with the entities of Ty table to find the corresponding location in Ty table (The entities in Ty table can either be in ascending or descending sequence), and then calculate the linear conversion according to the located section of Ty and Tx table.

When the source data is out of all entities of table, OVR=1.

It wouldn't execute this instruction if illegal SI or TI.

FUN34 P MLC	Multiple Linear Conversion (MLC)	FUN34 P MLC
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Expression:

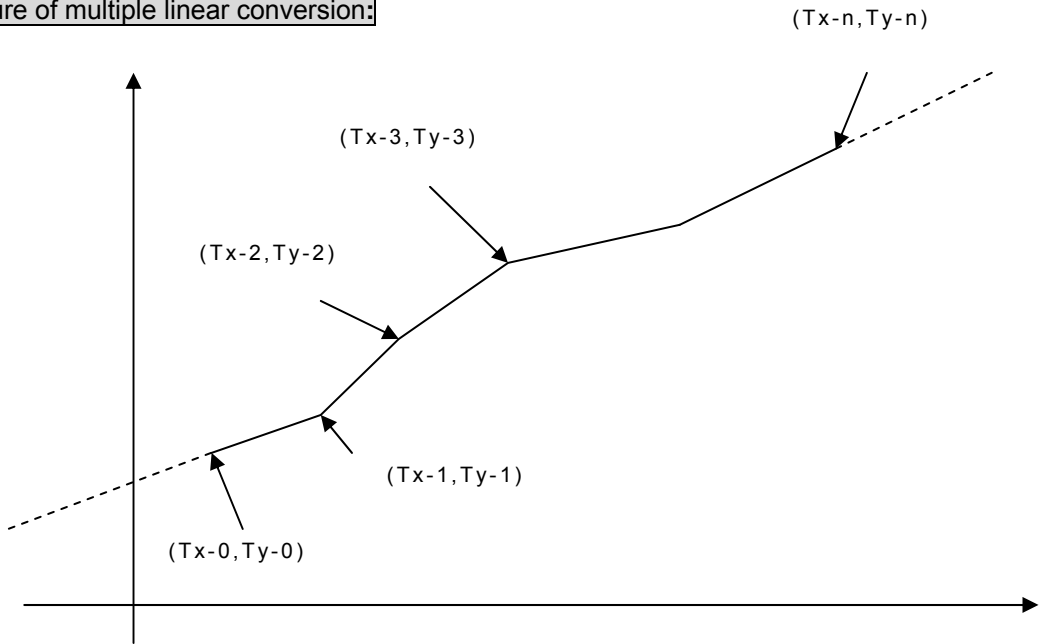
. The entities of Tx conversion parameter table must be in ascending sequence to have correct linear conversion; the entities of Ty conversion parameter table can either be in ascending or descending sequence. When executing this instruction, it will search the located section by comparing entities of the table with source data, and then calculate the linear conversion according to the following expression:

$$Vy = (Vx - Tx_n) \times (Ty_n+1 - Ty_n / Tx_n+1 - Tx_n) + Ty_n \text{ if } X/Y=0$$

$$Vx = (Vy - Ty_n) \times (Tx_n+1 - Tx_n / Ty_n+1 - Ty_n) + Tx_n \text{ if } X/Y=1$$

.Value of Vy、Vx、Tx_n、Tx_n+1、Ty_n、Ty_n+1 must be -32768~32767

Figure of multiple linear conversion:



Multiple Linear Conversion

FUN34 P
MLC

Multiple Linear Conversion
(MLC)

FUN34 P
MLC

Example 1 :

NO02

M10

M11

EN

X/Y

34.MLC

Rs: R0

S1: R99

Tx: R1000

Ty: R2000

T1: R199

D : D0

1000

6

0

0

5

140

OVR

M100

Description : When M10=1、M11=0, R0 is the starting address of source data、R99 is the quantity of source data, R1000 is the starting address of Tx conversion parameter table, R2000 is the starting address of Ty conversion parameter table、R199 is the quantity of table; the source data R0~R5 will be calculated the linear conversion according to Tx and Ty table between four sections, then store the results into D0~D5.

Status Monitoring

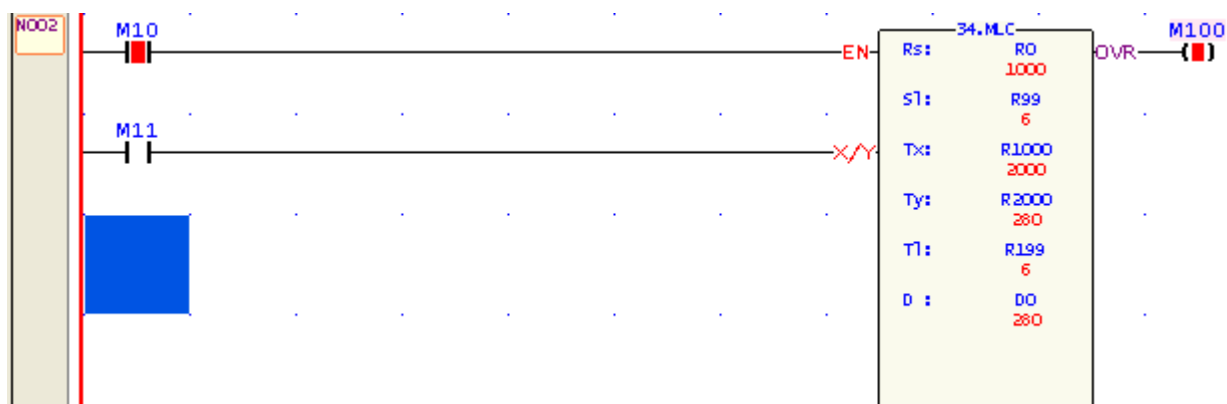
Ref. No.	Status	Data	Ref. No.	Status	Data	Ref. No.	Status	Data	Ref. No.	Status	Data
R1000	Decimal	0	R2000	Decimal	0	R0	Decimal	1000	D0	Decimal	140
R1001	Decimal	2000	R2001	Decimal	280	R1	Decimal	2500	D1	Decimal	342
R1002	Decimal	4000	R2002	Decimal	530	R2	Decimal	5600	D2	Decimal	714
R1003	Decimal	6000	R2003	Decimal	760	R3	Decimal	7500	D3	Decimal	917
R1004	Decimal	8000	R2004	Decimal	970	R4	Decimal	8000	D4	Decimal	970
R199	Decimal	5				R5	Decimal	10000	D5	Decimal	1180
M10	Enable	ON	M11	Enable	OFF	R99	Decimal	6			

StatusPage0 / StatusPage01 / StatusPage2

X	Y
0	0
2000	280
4000	530
6000	760
8000	970

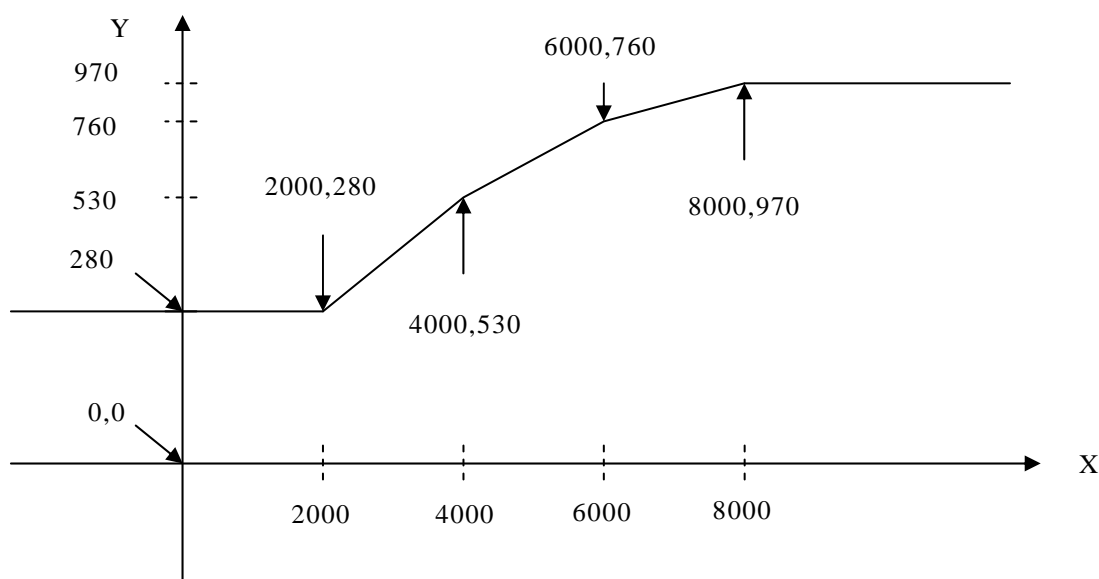
FUN34 P
MLCMultiple Linear Conversion
(MLC)FUN34 P
MLC

Example 2 :



Description : When M10=1、M11=0, R0 is the starting address of source data、R99 is the quantity of source data, R1000 is the starting address of Tx conversion parameter table, R2000 is the starting address of Ty conversion parameter table、R199 is the quantity of table; the source data R0~R5 will be calculated the linear conversion according to Tx and Ty table between five sections, then store the results into D0~D5. The result value is 280 if source data ≤ 2000 ; the result value is 970 if source data ≥ 8000 .

Ref. No.	Status	Data	Ref. No.	Status	Data	Ref. No.	Status	Data	Ref. No.	Status	Data
R1000	Decimal	2000	R2000	Decimal	280	R0	Decimal	1000	D0	Decimal	280
R1001	Decimal	2000	R2001	Decimal	280	R1	Decimal	2000	D1	Decimal	280
R1002	Decimal	4000	R2002	Decimal	530	R2	Decimal	3800	D2	Decimal	505
R1003	Decimal	6000	R2003	Decimal	760	R3	Decimal	7500	D3	Decimal	917
R1004	Decimal	8000	R2004	Decimal	970	R4	Decimal	8000	D4	Decimal	970
R1005	Decimal	8000	R2005	Decimal	970	R5	Decimal	10000	D5	Decimal	970
R199	Decimal	6	R99	Decimal	6	M10	Enable	ON	M11	Enable	OFF



Multiple Linear Conversion

FUN34 P
MLC

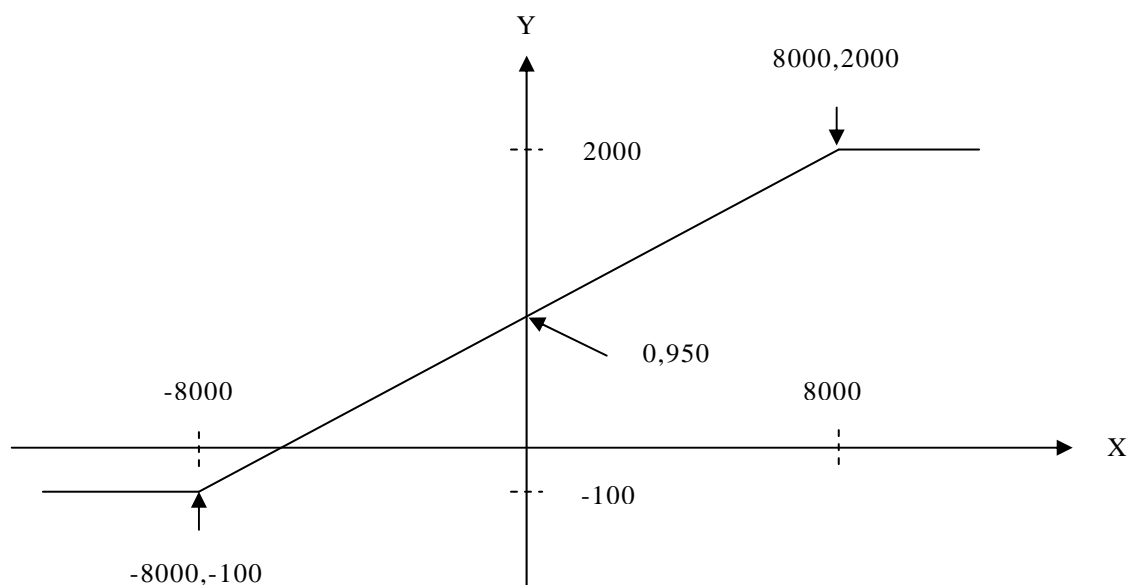
Multiple Linear Conversion
(MLC)

FUN34 P
MLC

Example 3 :

Ref. No.	Status	Data	Ref. No.	Status	Data	Ref. No.	Status	Data	Ref. No.	Status	Data
R1000	Decimal	-8000	R2000	Decimal	-100	R0	Decimal	-8100	D0	Decimal	-100
R1001	Decimal	-8000	R2001	Decimal	-100	R1	Decimal	0	D1	Decimal	950
R1002	Decimal	8000	R2002	Decimal	2000	R2	Decimal	4000	D2	Decimal	1475
R1003	Decimal	8000	R2003	Decimal	2000	R3	Decimal	8100	D3	Decimal	2000
R199	Decimal	4				R4	Decimal	-10000	D4	Decimal	-100
						R5	Decimal	10000	D5	Decimal	2000
M10	Enable	ON	M11	Enable	OFF	R99	Decimal	6			

Description : When M10=1、M11=0, R0 is the starting address of source data、R99 is the quantity of source data, R1000 is the starting address of Tx conversion parameter table, R2000 is the starting address of Ty conversion parameter table、R199 is the quantity of table; the source data R0~R5 will be calculated the linear conversion according to Tx and Ty table between three sections, then store the results into D0~D5. The result value is -100 if source data ≤ -8000 ; the result value is 2000 if source data ≥ 8000 .



FUN34 P
MLC

Multiple Linear Conversion
(MLC)

FUN34 P
MLC

Example 4 :

34.MLC

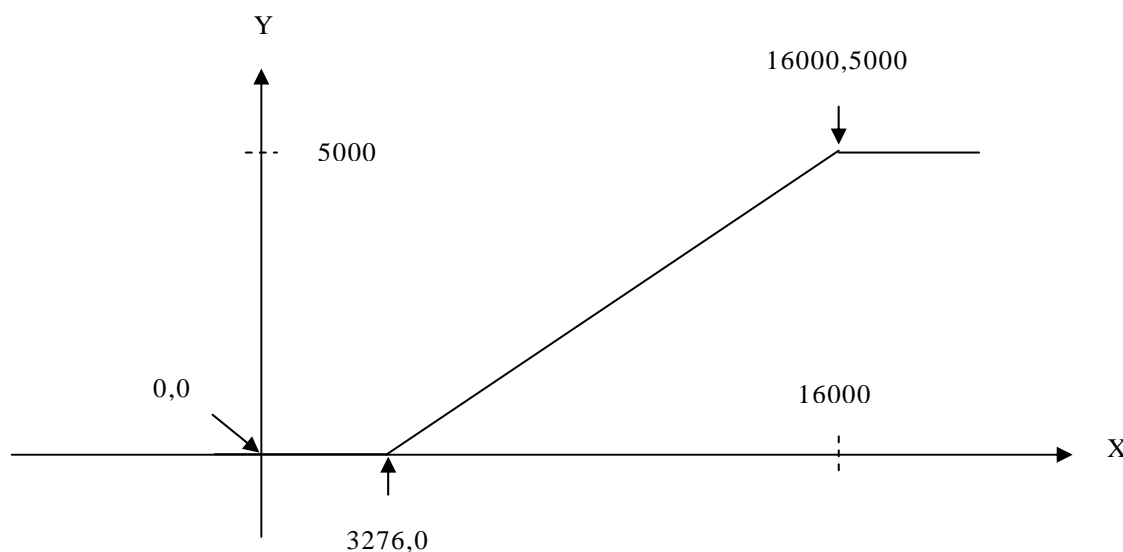
Rs: R0
S1: R99
Tx: R1000
Ty: R2000
T1: R199
D : D0

OVR → M100

Ref. No.	Status	Data	Ref. No.	Status	Data	Ref. No.	Status	Data	Ref. No.	Status	Data
R1000	Decimal	3276	R2000	Decimal	0	R0	Decimal	0	D0	Decimal	0
R1001	Decimal	3276	R2001	Decimal	0	R1	Decimal	3276	D1	Decimal	0
R1002	Decimal	16000	R2002	Decimal	5000	R2	Decimal	4095	D2	Decimal	321
R1003	Decimal	16000	R2003	Decimal	5000	R3	Decimal	9638	D3	Decimal	2500
R199	Decimal	4				R4	Decimal	16000	D4	Decimal	5000
						R5	Decimal	16380	D5	Decimal	5000
M10	Enable	ON	M11	Enable	OFF	R99	Decimal	6			

StatusPage0 / StatusPage01 / StatusPage2

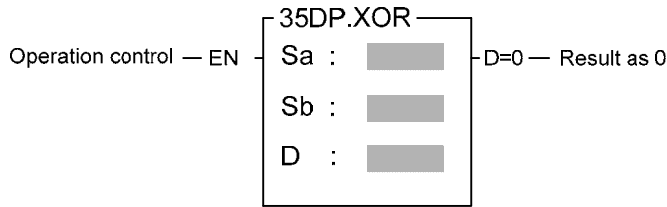
Description : When M10=1、M11=0, R0 is the starting address of source data、R99 is the quantity of source data, R1000 is the starting address of Tx conversion parameter table、R2000 is the starting address of Ty conversion parameter table、R199 is the quantity of table; the source data R0~R5 will be calculated the linear conversion according to Tx and Ty table between three sections, then store the results into D0~D5. The result value is 0 if source data ≤ 3276 ; the result value is 5000 if source data ≥ 16000 .



Logical Operation Instructions

FUN 35 D P XOR	EXCLUSIVE OR	FUN 35 D P XOR
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Ladder symbol



Sa : Source data a for exclusive or operation

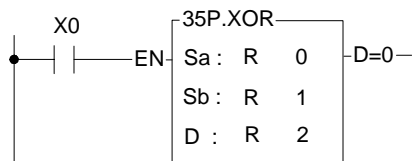
Sb : Source data b for exclusive or operation

D : Register storing XOR results

Sa, Sb, D may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	16/32bit +/- number	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9
Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>

- When operation control "EN" = 1 or changes from 0 to 1 (**P** instruction), will perform the logical XOR (exclusive or) operation of data Sa and Sb. The operation of this function is to compare the corresponding bits of Sa and Sb (B0~B15 or B0~B31), and if bits at the same position have different status, then set the corresponding bit within D as 1, otherwise as 0.
- After the operation, if all the bits in D are all 0, then set the 0 flag "D = 0" to 1.



- The instruction at left makes a logical XOR operation using the R0 and R1 registers, and stores the result in R2.

Sa	R0	1	0	1	1	1	0	1	1	0	1	1	0	1	1	0	1
Sb	R1	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0

⇓ X0 = ⇓

D	R2	0	1	0	1	0	1	0	1	1	1	0	0	1	0	1	1
---	----	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

FUN 36 **D** **P**
XNR

EXCLUSIVE NOR

FUN 36 **D** **P**
XNR

Ladder symbol

Operation control — EN

36DP.XNR

Sa :

Sb :

D :

D=0 — Result as 0

Sa : Data a for XNR operation

Sb : Data b for XNR operation

D : Register storing XNR results

Sa, Sb, D may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	16/32-bit ± number	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9
Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>

●

When operation control "EN" = 1 or changes from 0 to 1 (**P** instruction), will perform the logical XNR (inclusive or) operation of data Sa and Sb. The operation of this function is to compare the corresponding bits of Sa and Sb (B0~B15 or B1~B31), and if the bit has the same value, then set the corresponding bit within D as 1. If not then set it to 0.

●

After the operation, if the bits in D are all 0, then set the 0 flag "D=0" to 1.

X0

●

—

—

—

EN

36P.XNR

Sa : R 0

Sb : R 1

D : R 2

D=0—

●

The instruction at left makes a logical XNR operation of the R0 and R1 registers, and the results are stored in the R2 register.

Sa

R0	1	0	1	1	1	0	1	1	0	1	1	0	1	1	0	1
----	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Sb

R1	1	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0
----	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---












⇓ X0=

D

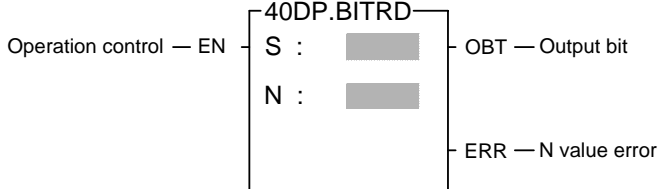
R2	1	0	1	0	1	0	1	0	0	0	1	1	0	1	0	0
----	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

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Comparison Instructions

FUN 37  		ZONE COMPARE										FUN 37  																																																																																										
ZNCMP												ZNCMP																																																																																										
<div><div><div>Ladder symbol</div><div><div>37DP.ZNCMP</div><div><div>Operation control — EN</div><div><div>S : </div><div>INZ — Inside zone</div><div>Su : </div><div>S>U — Higher than upper limit</div><div>SL : </div><div>S<L — Lower than lower limit</div><div>ERR — Limit value erroe</div></div></div></div><div><div>S : Register for zone comparison</div><div>SU : The upper limit value</div><div>SL : The lower limit value</div><div>S, SU, SL may combine with V, Z, P0~P9 to serve indirect address application</div></div></div></div>																																																																																																						
<table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><th rowspan="2">Ope- rand</th><td>WX0</td><td>WY0</td><td>WM0</td><td>WS0</td><td>T0</td><td>C0</td><td>R0</td><td>R3840</td><td>R3904</td><td>R3968</td><td>R5000</td><td>D0</td><td>16/32-bit +/- number</td><td>V · Z</td></tr><tr><td>WX240</td><td>WY240</td><td>WM1896</td><td>WS984</td><td>T255</td><td>C255</td><td>R3839</td><td>R3903</td><td>R3967</td><td>R4167</td><td>R8071</td><td>D4095</td><td></td><td>P0~P9</td></tr><tr><td>S</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td></tr><tr><td>Su</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr><tr><td>SL</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr></table>														Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	16/32-bit +/- number	V · Z	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9	S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	Su	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	SL	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR																																																																																								
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	16/32-bit +/- number	V · Z																																																																																								
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9																																																																																								
S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>																																																																																								
Su	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																																																																																								
SL	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																																																																																								
<ul style="list-style-type: none">When operation control "EN" = 1 or changes from 0 to 1 ( instruction), compares S with upper limit Su and lower limit SL. If S is between the upper limit and the lower limit ($S_L \leq S \leq S_U$), then set the inside zone flag "INZ" to 1. If the value of S is greater than the upper limit S_U, then set the higher than upper limit flag "S>U" to 1. If the value of S is smaller then the lower limit S_L, then set the lower than lower limit flag "S<L" as 1.The upper limit S_U should be greater than the lower limit S_L. If $S_U < S_L$, then the limit value error flag "ERR" will set to 1, and this instruction will not carry out.																																																																																																						
<div><div><div><div>X0</div><div><div>37P.ZNCMP</div><div><div>EN</div><div><div>S : R 0</div><div>Su : R 1</div><div>SL : R 2</div></div></div></div><div><div>Y0</div><div>()</div><div>S>U—</div><div>S<L—</div><div>ERR—</div></div></div></div><div><ul style="list-style-type: none">The instruction at left compares the value of R0 with the upper and lower limit zones formed by R1 and R2. If the values of R0~R2 are as shown in the diagram at bottom left, then the result can then be obtained as at the right of this diagram.If want to get the status of out side the zone, then OUT NOT Y0 may be used, or an OR operation between the two outputs S>U and S<L may be carried out, and move the result to Y0.</div></div>																																																																																																						
<div><div><div><div>S</div><div>Su</div><div>SL</div></div><div><table><tr><td>R0</td><td>200</td></tr><tr><td>R1</td><td>300</td></tr><tr><td>R2</td><td>100</td></tr></table></div><div><div>(Upper limit value)</div><div>(Lower limit value)</div></div></div><div><div>X0 = </div><div></div></div><div><div>Y0</div><div></div><div>Results of execution</div></div><div>Before-execution</div></div>														R0	200	R1	300	R2	100																																																																																			
R0	200																																																																																																					
R1	300																																																																																																					
R2	100																																																																																																					

FUN 40 D P BITRD	BIT READ	FUN 40 D P BITRD
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Ladder symbol

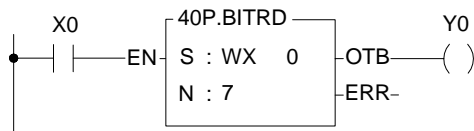
S : Source data to be read

N : The bit number of the S data to be read out.

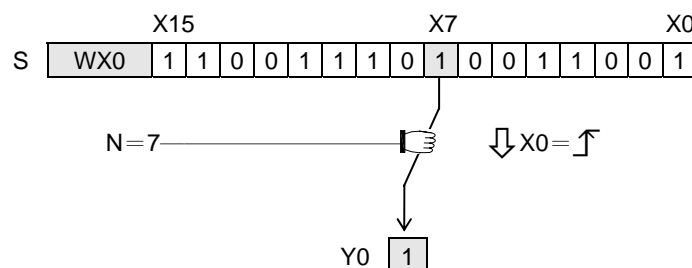
S, N may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number	V · Z P0~P9
	○	○	○	○	○	○	○	○	○	○	○	○	○	○
S	○	○	○	○	○	○	○	○	○	○	○	○	○	○
N	○	○	○	○	○	○	○	○	○	○	○	○	0~31	○

- When read control "EN" = 1 or changes from 0 to 1 (**P** instruction), take the Nth bit of the S data out , and put it to the output bit "OTB".
- When read control "EN" = 0, the output "OTB" can be selected to keep at the last state (if M1919=0) or set to zero (if M1919=1).
- When the operand is 16 bit, the effective range for N is 0~15. For 32 bit operand (**D** instruction) it is 0~31. N beyond this range will set the N value error flag "ERR" to 1, and do not carry out this instruction.



- The instruction at left reads the 7th bit (X7) status from WX0 (X0~X15) and output to Y0. The results are as follows:



FUN 41 D P BITWR	BIT WRITE	FUN 41 D P BITWR
-----------------------------------	-----------	-----------------------------------

Ladder symbol

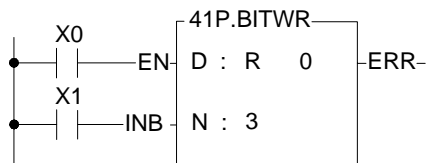
D : Register for bit write

N : The bit number of the D register to be written.

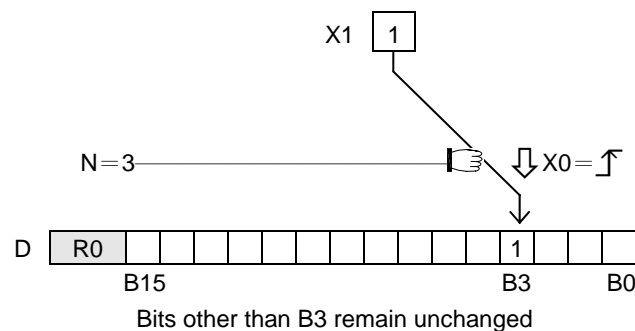
D, N may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	0 0	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	15 31	P0~P9
D														
N														

- When write control "EN" = 1 or changes from 0 to 1 (**P** instruction), will write the write bit (INB) into the Nth bit of register D.
- When the operand is 16 bit, the effective range of N is 0~15. For 32 bit (**D** instruction) operand it is 0~31. N beyond this range, will set the N value error flag "ERR" to 1, and do not carry out this instruction.



- The instruction at left writes the status of the write bit INB into B3 of R0. Assuming X1 = 1, the result will be as follows:



FUN 42 D P BITMV		BIT MOVE														FUN 42 D P BITMV	
<div><div><div><div><div></div><div></div><div></div><div></div></div><div><div></div><div></div><div></div><div></div></div></div><div><div></div><div></div><div></div><div></div></div></div><div><div></div><div></div><div></div><div></div></div></div> <div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div></div> <div><div></div><div></div><div></div><div></div></div> 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FUN 43 **D** **P**
NBMV

NIBBLE MOVE

FUN 43 **D** **P**
NBMV

Ladder symbol

43DP.NBMV

Move control — EN

S :

Ns :

D :

Nd :

ERR — N value error

S : Source data to be moved

Ns: Assign Ns nibble within S as source nibble

D : Destination register to be moved

Nd: Assign Nd nibble within D as target nibble

S, Ns, D, Nd may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	16/32-bit +/- number	V、Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9
S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Ns	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	0~7	<input type="radio"/>
D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>
Nd	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	0~7	<input type="radio"/>

X0

EN

43P.NBMV

S : R 0

Ns : 2

D : R 1

Nd : 1

ERR—

● The instruction at left moves the third nibble NB2 (B8~B11) within S to the first nibble NB1 (B4~B7) within D. Other nibbles within D remain unchanged.

S

R0

B15

B0

NB3

NB2

NB1

NB0

Ns=2

Nd=1

D

R1

B15

B0

NB3

NB2

NB1

NB0

↴ X0=↵

7-31

FUN 44 D P BYMV	BYTE MOVE	FUN 44 D P BYMV
----------------------------------	-----------	----------------------------------

Ladder symbol

44DP.BYMV
 Move control — EN — S : — ERR — N value error
 Ns :
 D :
 Nd :

S : Source data to be moved

Ns : Assign Ns byte within S as source byte

D : Destination register to be moved

Nd : Assign Nd byte within D as target byte

S, Ns, D, Nd may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	16/32-bit +/- number	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9
S	○	○	○	○	○	○	○	○	○	○	○	○	○	○
Ns	○	○	○	○	○	○	○	○	○	○	○	○	0~3	○
D		○	○	○	○	○	○		○	○*	○*	○		○
Nd	○	○	○	○	○	○	○	○	○	○	○	○	0~3	○

- When move control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), move Nsth byte within S to Ndth byte position within D. (A byte is comprised of 8 bits. Starting from the lowest bit of the register, B0, each successive eight bits form a byte, so B0~B7 form byte 0, B8~B15 form byte 1, etc...)
- When the operand is 16 bit, the effective range of Ns or Nd is 0~1. For 32 bit (**D** instruction) operand, the range is 0~3. Beyond this range, will set the N value error flag "ERR" to 1, and do not carry out this instruction.

Ladder symbol

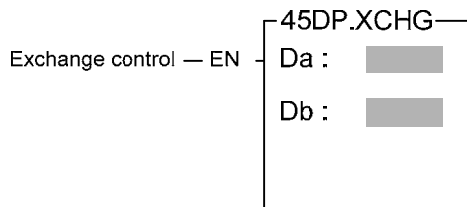
44DP.BYMV
 X0 — EN — S : R 0 — ERR—
 Ns : 2
 D : R 2
 Nd : 1

- The instruction at left moves the third byte (B16~B23) within S (32 bit register composed of R1R0), to the first byte within D (32 bit register composed of R3R2). Other bytes within D remain unchanged.

X0 = 1

FUN 45 D P XCHG	EXCHANGE	FUN 45 D P XCHG
----------------------------------	----------	----------------------------------

Ladder symbol



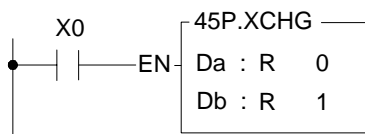
Da : Register a to be exchanged

Db : Register b to be exchanged

Da, Db may combine with V, Z, P0~P9 to serve indirect address application

Range	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	XR
Ope- rand	WY0	WM0	WS0	T0	C0	R0	R3904	R3968	R5000	D0	V · Z
	WY240	WM1896	WS984	T255	C255	R3839	R3967	R4167	R8071	D4095	P0~P9
Da	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Db	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

- When exchange control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), will exchanges the contents of register Da and register Db in 16 bits or 32 bits (**D** instruction) format.



- The instruction at left exchanges the contents of the 16-bit R0 and R1 registers.

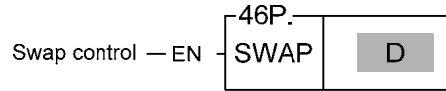
		B15														B0					
Da	R0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Db	R1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

⇓ X0 = ⇓

		B15														B0					
Da	R0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Db	R1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FUN 46 **P**
SWAP

BYTE SWAP

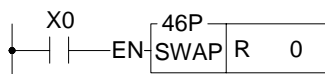
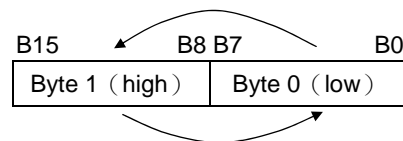
FUN 46 **P**
SWAPLadder symbol

D : Register for byte data swap

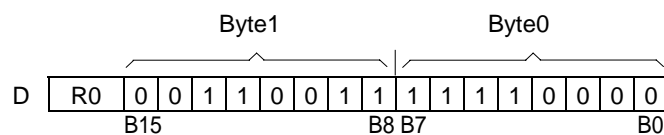
D may combine with V, Z, P0~P9 to serve indirect address application

Range	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	XR
Ope- rand	WY0	WM0	WS0	T0	C0	R0	R3904	R3968	R5000	D0	V · Z
	WY240	WM1896	WS984	T255	C255	R3839	R3967	R4167	R8071	D4095	P0~P9
D	○	○	○	○	○	○	○	○*	○*	○	○

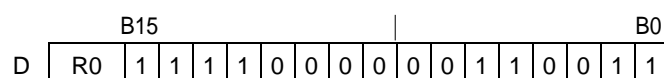
- When swap control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), swap the data of the low byte, Byte 0 (B0~B7), and the high byte, Byte 1 (B8~B15), in the 16 bit register specified by D.



- The instruction at left swaps the data of the low byte (B0~B7) and the high byte (B8~B15) in R0. The results are as follows:



⇓ X0 = ⌈



FUN 47 P UNIT	NIBBLE UNITE	FUN 47 P UNIT
-------------------------	--------------	-------------------------

Ladder symbol

Unite control — EN

47P.UNIT
 S :
 N :
 D :

ERR — N value error

S : Starting source register to be united

N : Number of nibbles to be united

D : Registers storing united data

S, N, D may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	1	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	4	P0~P9
S	○	○	○	○	○	○	○	○	○	○	○	○		○
N	○	○	○	○	○	○	○	○	○	○	○	○	○	○
D		○	○	○	○	○	○		○	○*	○*	○		○

- When unite control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), take out the lowest nibbles NB0, of N successive registers starting from S, and fill them into NB0, NB1,NBn-1 of D in ascending order. Nibbles not yet filled in D (when N is odd) are filled with 0. (A nibble is comprised by 4 bits. Starting from the lowest bit in the register, B0, each successive four bits form a nibble, so B0~B3 form nibble 0, B4~B7 form nibble 1, etc...).
- This instruction only provides WORD (16 bit) operand. Because of this, there are usually only 4 nibbles can be involved. Therefore the effective range of N is 1~4. Beyond this range, will set the N value error flag "ERR" to 1, and do not carry out this instruction.

X0 — EN

47P.UNIT
 S : R 0
 N : 3
 D : WY 0

ERR—

● The instruction at left takes out NB0 from 3 registers, R0, R1 and R2, and fills them into NB0~NB2 within WY0 register.

N=3

	B15	B12	B11	B8	B7	B4	B3	B0
S	R0							0001
S+1	R1							0010
S+2	R2							0100

NB3 NB2 NB1 NB0

N=3

	NB3	NB2	NB1	NB0
D	WY0	0000	0100	0001

Y15 ↑ Y0 ↑

Set the not united NB as 0

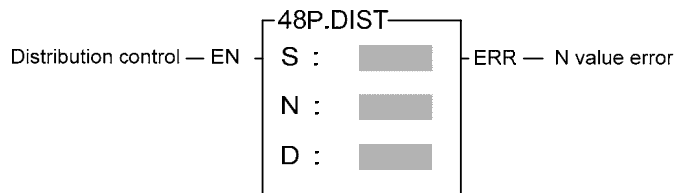
X0 =

FUN 48 **P**
DIST

NIBBLE DISTRIBUTE

FUN 48 **P**
DIST

Ladder symbol



S : Source data to be distributed

N : Number of nibbles to be distributed

D : Starting register storing distribution data

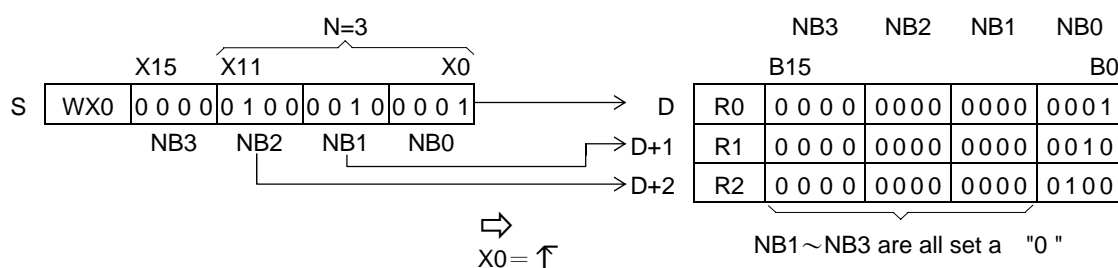
S, N, D may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Operand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	16-bit +/- number	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9
S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
N	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	1~4	<input type="radio"/>
D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>

- When distribution control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), will take N successive nibbles starting from the lowest nibble NB0 within S, and distribute them in ascending order into the 0 nibbles of N registers starting from D. The nibbles other than NB0 in each of the registers within D are all set to zero. (A nibble is comprised by 4 bits. Starting from the lowest bit in a register, B0, each successive 4 bits form a nibble, so B0~B3 form nibble 0, B4~B7 form nibble 1, etc...)
- This instruction only provides WORD (16 bit) operand. Therefore there are usually only 4 nibbles can be involved, so the effective value of N is 1~4. Beyond this range, will set the N value error flag "ERR" to 1, and do not carry out this instruction.



- The instruction at left writes NB0~NB2 from the WX0 register into the NB0 of the 3 consecutive registers R0~R2.



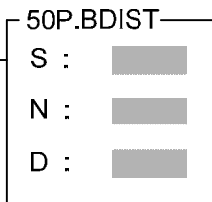
FUN49 P BUNIT	BYTE UNITE	FUN49 P BUNIT																																																																						
<div><div><div>Ladder symbol</div><div><div>Execution control — EN</div><div><div>49P.BUNIT</div><div>S : <div></div></div><div>N : <div></div></div><div>D : <div></div></div></div></div><div><div>S : Starting address of source register to be united</div><div>N : Number of bytes to be united</div><div>D : Registers to store the united data</div><div>S, N, D may associate with V、Z、P0~P9 index register to serve the indirect addressing application</div></div><div><table><tr><th>Range</th><th>HR</th><th>ROR</th><th>DR</th><th>K</th></tr><tr><td>Ope- rand</td><td>R0 R3839</td><td>R5000 R8071</td><td>D0 D4095</td><td></td></tr><tr><td>S</td><td><div></div></td><td><div></div></td><td><div></div></td><td></td></tr><tr><td>N</td><td><div></div></td><td><div></div></td><td><div></div></td><td>1~256</td></tr><tr><td>D</td><td><div></div></td><td><div></div>*</td><td><div></div></td><td></td></tr></table></div></div><div><div><div>● When execution control "EN"=1 or changes from 0→1 P instruction, it will perform the byte combination starting from S, length by N, and then store the results into D registers.</div><div>● This instruction will not act if invalid range of length.</div><div>● When communicating with intelligent peripheral in binary data format, this instruction may be applied to do byte combination for following word data processing.</div></div><div><div>Example :</div><div><div><div>M2</div><div><div></div><div></div></div><div>EN</div></div><div><div>49P.BUNIT</div><div>S : R 1500</div><div>N : R 999</div><div>D : R 2500</div></div></div><div><div>Description : When M2 changes from 0→1, it will perform the byte combination starting from R1500, the length is assigned by R999, and then store the results into registers starting from R2500.</div><div>It is supposed R999=10, the results of combination will store into R2500~R2504.</div><div><div><div>S</div><div><div>High Byte</div><div>Low Byte</div></div><div><table><tr><td>R1500</td><td>Don't care</td><td>Byte-0</td></tr><tr><td>R1501</td><td>Don't care</td><td>Byte-1</td></tr><tr><td>R1502</td><td>Don't care</td><td>Byte-2</td></tr><tr><td>R1503</td><td>Don't care</td><td>Byte-3</td></tr><tr><td>R1504</td><td>Don't care</td><td>Byte-4</td></tr><tr><td>R1505</td><td>Don't care</td><td>Byte-5</td></tr><tr><td>R1506</td><td>Don't care</td><td>Byte-6</td></tr><tr><td>R1507</td><td>Don't care</td><td>Byte-7</td></tr><tr><td>R1508</td><td>Don't care</td><td>Byte-8</td></tr><tr><td>R1509</td><td>Don't care</td><td>Byte-9</td></tr></table></div></div><div><div>D</div><div><div>High Byte</div><div>Low Byte</div></div><div><table><tr><td>R2500</td><td>Byte-0</td><td>Byte-1</td></tr><tr><td>R2501</td><td>Byte-2</td><td>Byte-3</td></tr><tr><td>R2502</td><td>Byte-4</td><td>Byte-5</td></tr><tr><td>R2503</td><td>Byte-6</td><td>Byte-7</td></tr><tr><td>R2504</td><td>Byte-8</td><td>Byte-9</td></tr></table></div></div></div></div></div></div></div>			Range	HR	ROR	DR	K	Ope- rand	R0 R3839	R5000 R8071	D0 D4095		S	<div></div>	<div></div>	<div></div>		N	<div></div>	<div></div>	<div></div>	1~256	D	<div></div>	<div></div> *	<div></div>		R1500	Don't care	Byte-0	R1501	Don't care	Byte-1	R1502	Don't care	Byte-2	R1503	Don't care	Byte-3	R1504	Don't care	Byte-4	R1505	Don't care	Byte-5	R1506	Don't care	Byte-6	R1507	Don't care	Byte-7	R1508	Don't care	Byte-8	R1509	Don't care	Byte-9	R2500	Byte-0	Byte-1	R2501	Byte-2	Byte-3	R2502	Byte-4	Byte-5	R2503	Byte-6	Byte-7	R2504	Byte-8	Byte-9
Range	HR	ROR	DR	K																																																																				
Ope- rand	R0 R3839	R5000 R8071	D0 D4095																																																																					
S	<div></div>	<div></div>	<div></div>																																																																					
N	<div></div>	<div></div>	<div></div>	1~256																																																																				
D	<div></div>	<div></div> *	<div></div>																																																																					
R1500	Don't care	Byte-0																																																																						
R1501	Don't care	Byte-1																																																																						
R1502	Don't care	Byte-2																																																																						
R1503	Don't care	Byte-3																																																																						
R1504	Don't care	Byte-4																																																																						
R1505	Don't care	Byte-5																																																																						
R1506	Don't care	Byte-6																																																																						
R1507	Don't care	Byte-7																																																																						
R1508	Don't care	Byte-8																																																																						
R1509	Don't care	Byte-9																																																																						
R2500	Byte-0	Byte-1																																																																						
R2501	Byte-2	Byte-3																																																																						
R2502	Byte-4	Byte-5																																																																						
R2503	Byte-6	Byte-7																																																																						
R2504	Byte-8	Byte-9																																																																						

FUN50 **P**
BDIST

BYTE DISTRIBUTE

FUN50 **P**
BDISTLadder symbol

Execution control — EN



S : Starting address of source register to be distributed

N : Number of bytes to be distributed

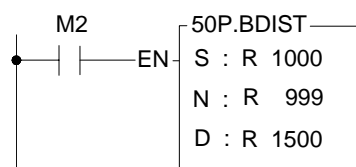
D : Registers to store the distributed data

S, N, D may associate with V·Z·P0~P9 index register to serve the indirect addressing application.

Range	HR	ROR	DR	K
Ope- rand	R0 R3839	R5000 R8071	D0 D4095	
S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	
N	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	1~256
D	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	

- When execution control "EN" =1 or changes from 0→1 (**P** instruction), it will perform the byte distribution starting from S, length by N, and then store the results into D registers.
- This instruction will not act if invalid range of length.
- When communicating with intelligent peripheral in binary data format, this instruction may be applied to do byte distribution for data transmission °

Example :



Description : When M2 changes from 0→1, it will perform the byte distribution starting from R1000, the length is assigned by R999, and then store the results into registers starting from R1500.

It is supposed R999=9, the results of distribution will store into R1500~R1508.

	S	
	High Byte	Low Byte
R1000	Byte-0	Byte-1
R1001	Byte-2	Byte-3
R1002	Byte-4	Byte-5
R1003	Byte-6	Byte-7
R1004	Byte-8	Don't care

	D	
	High Byte	Low Byte
R1500	00	Byte-0
R1501	00	Byte-1
R1502	00	Byte-2
R1503	00	Byte-3
R1504	00	Byte-4
R1505	00	Byte-5
R1506	00	Byte-6
R1507	00	Byte-7
R1508	00	Byte-8

Shifting/Rotating Instructions

FUN 51 D P SHFL	SHIFT LEFT	FUN 51 D P SHFL
---------------------------	------------	---------------------------

Ladder symbol

Shift control — EN

Shift in bit — INB

51DP.SHFL

D :

N :

OTB — Shift-out bit

ERR — N value error

D : Register to be shifted

N : Number of bits to be shifted

N, D may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	1 1	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	16 or 32	P0~P9
D		○	○	○	○	○	○		○	○*	○*	○		○
N	○	○	○	○	○	○	○	○	○	○	○	○	○	○

- When shift control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), will shift the data of the D register towards the left by N successive bits (in ascending order). After the lowest bit B0 has been shifted left, its position will be replaced by shift-in bit INB, while the status of shift-out bits B15 or B31 (**D** instruction) will appear at shift-out bit "OTB".
- If the operand is 16 bit, the effective range of N is 1~16. For 32 bits (**D** instruction) operand, it is 1~32. Beyond this range, will set the N value error flag "ERR" to 1, and do not carry out this instruction.

X0

INB

51P.SHFL

D : R 0

N : 4

Y0

OTB — ()

ERR—

- The instruction at left shifts the data in register R0 towards the left by 4 successive bits. The results are shown below.

Y0

B15

R0

B0

0

0

1

1

0

0

1

0

1

1

1

1

0

0

0

0

*

⇩ X0 = ⇧

Y0

B15

R0

B0

0

0

1

0

1

1

1

1

0

0

0

0

1

1

1

1

* △ △ △ △

7-39

FUN 52 **D** **P**
SHFR

SHIFT RIGHT

FUN 52 **D** **P**
SHFR

Ladder symbol

Shift control — EN

Shift in bit — INB

52DP.SHFR

D :

N :

OTB — Shift-out bit

ERR — N value error

D : Register to be shifted

N : Number of bits to be shifted

D, N may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	1 1	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	16 or 32	P0~P9
D		○	○	○	○	○	○		○	○*	○*	○		○
N	○	○	○	○	○	○	○	○	○	○	○	○	○	○

- When shift control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), will shift the data of D register towards the right by N successive bits (in descending order). After the highest bits, B15 or B31 (**D** instruction) have been shifted right, their positions will be replaced by the shift-in bit INB, while shift-out bit B0 will appear at shift-out bit "OTB".
- If the operand is 16 bit, the effective range of N is 1~16. For 32 bits (**D** instruction) operand, it is 1~32. Beyond this range, will set the N value error flag "ERR" to 1, and do not carry out this instruction.

X0

EN

52P.SHFR

D : R 0

N : 15

OTB — ()

ERR —

INB

The instruction at left shifts the data in R0 register towards the right by 15 successive bits. The results are shown below.

INB

0

→

B15

1

0

1

0

1

0

1

0

1

0

1

0

1

0

1

0

→

B0

0

→

Y0

△

*

⇓ X0 = ⇑

INB

0

→

B15

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

1

→

Y0

0

△

△

△

△

△

△

△

△

△

△

△

△

△

△

△

△

*

7-40

Shifting/Rotating Instructions

FUN 53 **D** **P**
ROTL

ROTATE LEFT

FUN 53 **D** **P**
ROTL

Ladder symbol

53DP.ROTL

Rotate control — EN — **D** :

N :

OTB — Rotate-out-bit

ERR — N value error

D : Register to be rotated

N : Number of bits to be rotated

D, N may combine with V, Z , P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	1 or 16	1 or 32
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9
D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>
N	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

● When rotate control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), will rotate the data of D register towards the left by N successive bits (in ascending order, ie. in a 16-bit instruction, B0→B1, B1→B2, , B14→B15, B15→B0. In a 32-bit instruction, B0→B1, B1→B2, , B30→B31, B31→B0). At the same time, the status of the rotated out bits B15 or B31 (**D** instruction) will appear at rotate-out bit "OTB".

● If the operand is 16 bit, the effective range of N is 1~16. For 32 bits (**D** instruction) operand, it is 1~32. Beyond this range, will set the N value error flag "ERR" to 1, and do not carry out this instruction.

X0

EN

53P.ROTL

D : R 0

N : 9

OTB — ()

ERR—

Y0

R0

B0

1 1 1 1 0 0 0 0 1 0 1 0 1 0 1 0

*

Y0

X0=

Y0

1 0 1 0 1 0 1 1 1 1 0 0 0 0 1

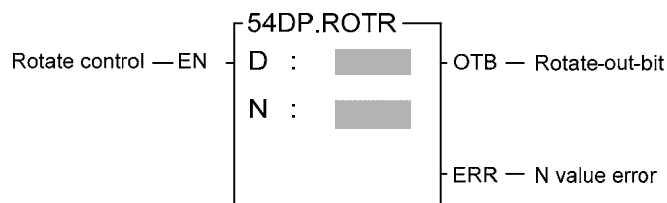
*

Y0

● The instruction at left rotates data from the R0 register towards the left 9 successive bits. The results are shown below.

7-41

FUN 54 D P ROTR	ROTATE RIGHT	FUN 54 D P ROTR
----------------------------------	--------------	----------------------------------

Ladder symbol

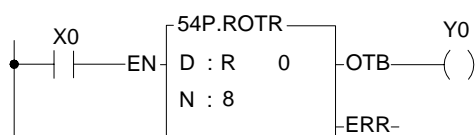
D : Register to be rotated

N : Number of bits to be rotated

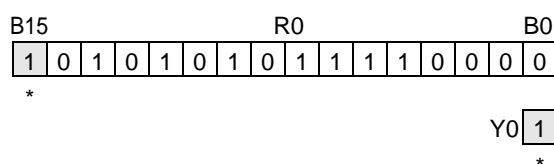
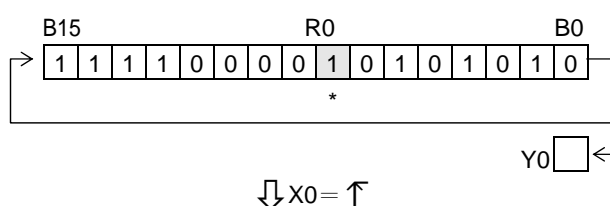
D, N may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	1 16 or 32	V - Z P0~P9
D		○	○	○	○	○	○		○	○*	○*	○		○
N	○	○	○	○	○	○	○	○	○	○	○	○	○	○





- When rotate control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), will rotate the bit data of D register towards the right by N successive bits (in descending order, ie. in a 16-bit instruction, B15→B14, B14→B13, ..., B1→B0, B0→B15. In a 32-bit instruction, B31→B30, B30→B29, ..., B1→B0, B0→B31). At the same time, the status of the rotated out B0 bits will appear at the rotate-out bit "OTB".
- If the operand is 16 bit, the effective range of N is 1~16. For 32 bits (**D** instruction) operand, it is 1~32. Beyond this range, will set the N value error flag "ERR" to 1, and do not carry out this instruction.



- The instruction at left rotates data from R0 register towards the right 8 successive bits. The results are shown below.







FUN55 D P B→G		BINARY-CODE TO GRAY-CODE CONVERSION												FUN55 D P B→G																																																												
<div><div>Ladder symbol</div><div>Operation control — EN<div>55DP.B→G<div>S : <div></div>D : <div></div></div></div></div></div>																<div>S : Starting of source</div> <div>D : Starting address of destination</div> <div>S , D operand can combine V 、 Z 、 P0~P9 for index addressing</div>																																																										
<table><tr><td rowspan="3">Range Ope- rand</td><td>WX</td><td>WY</td><td>WM</td><td>WS</td><td>TMR</td><td>CTR</td><td>HR</td><td>IR</td><td>OR</td><td>SR</td><td>ROR</td><td>DR</td><td>K</td><td>XR</td></tr><tr><td>WX0 WX240</td><td>WY0 WY240</td><td>WM0 WM1896</td><td>WS0 WS984</td><td>T0 T255</td><td>C0 C255</td><td>R0 R3839</td><td>R3840 R3903</td><td>R3904 R3967</td><td>R3968 R4167</td><td>R5000 R8071</td><td>D0 D4095</td><td>16/32-bit +/- number</td><td>V 、 Z P0~P9</td></tr><tr><td>S</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td></tr><tr><td>D</td><td></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td></tr></table>		Range Ope- rand	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number	V 、 Z P0~P9	S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>														
Range Ope- rand	WX		WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR																																																											
	WX0 WX240		WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number	V 、 Z P0~P9																																																											
	S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>																																																											
D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>																																																												
<div><div><div><div>●</div><div>When operation control "EN"=1 or changes from 0→1(P instruction), it will perform the code conversion; where S is the source (Binary code), and D is the destination (Gray code) for storing the result.</div></div><div><div>●</div><div>The conversion method shown as below</div></div></div><div><div><div>XOR XOR XOR XOR XOR XOR XOR XOR XOR XOR XOR XOR XOR XOR XOR</div><div><div>1 0 0 1 1 0 0 0 1 1 1 0 1 1 0 1</div><div><div>↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓</div><div>→1 1 0 1 0 1 0 0 1 0 0 1 1 0 1 1</div></div></div></div></div><div><div>Example 1: When M0 changes from 0→1, it will perform the 16-bit code conversion</div><div><div><div>M0<div>• — EN<div>55P.B→G<div>S : R0D : R100</div></div></div></div><div><div>●</div><div>Converting the 16-bit Binary-code in R0 into Gray-code, and then storing the result into R100.</div></div></div><div><div>R0= 1001010101010011B → R100= 110111111111010B</div></div></div></div></div>																																																																										

FUN55   B→G	BINARY-CODE TO GRAY-CODE CONVERSION	FUN55   B→G
<p>Example 2: When M0 =1, it will perform the 32-bit code conversion</p> <div><div><div>M0</div><div><div></div><div></div></div><div>EN</div></div><div><div>55DP.B→G</div><div>S : R0</div><div>D : R100</div></div></div> <ul style="list-style-type: none">• Converting the 32-bit Binary-code in DR0 into Gray-code, and then storing the result into DR100. <p>DR0 = 00110111001001000010111100010100B → DR100 = 00101100101101100011100010011110B</p>		

Code Conversion Instructions

FUN56 D P G→B		GRAY-CODE TO BINARY-CODE CONVERSION												FUN56 D P G→B	
<div><div>Ladder symbol</div><div><div>56DP.G→B</div><div><div>Operation control — EN</div><div><div>S : <div></div></div><div>D : <div></div></div></div></div></div><div><div>S : Starting of source</div><div>D : Starting address of destination</div><div>S , D operand can combine V 、 Z 、 P0~P9 for index addressing</div></div></div>															
<div><div>Range</div><div>WX</div><div>WY</div><div>WM</div><div>WS</div><div>TMR</div><div>CTR</div><div>HR</div><div>IR</div><div>OR</div><div>SR</div><div>ROR</div><div>DR</div><div>K</div><div>XR</div></div>		<div><div>WX0</div><div>WY0</div><div>WM0</div><div>WS0</div><div>T0</div><div>C0</div><div>R0</div><div>R3840</div><div>R3904</div><div>R3968</div><div>R5000</div><div>D0</div><div>16/32-bit +/- number</div><div>V 、 Z</div></div>		<div><div>WX240</div><div>WY240</div><div>WM1896</div><div>WS984</div><div>T255</div><div>C255</div><div>R3839</div><div>R3903</div><div>R3967</div><div>R4167</div><div>R8071</div><div>D4095</div><div>P0~P9</div></div>		<div><div>S</div><div><div><div></div></div></div></div>		<div><div>D</div><div><div><div></div></div></div></div>							
<div><div><div>●</div><div>When operation control "EN"=1 or changes from 0→1 (P instruction), it will perform the code conversion; where S is the source (Gray code), and D is the destination (Binary code) for storing the result.</div></div><div><div><div>●</div><div>The conversion method shown as below :</div></div></div></div>															
<div><div><div><div>1</div><div>0</div><div>0</div><div>1</div><div>1</div><div>0</div><div>0</div><div>0</div><div>0</div><div>1</div><div>1</div><div>1</div><div>0</div><div>1</div><div>1</div><div>0</div><div>1</div></div><div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div><div>XOR</div></div><div><div>1</div><div>1</div><div>1</div><div>0</div><div>1</div><div>1</div><div>1</div><div>1</div><div>0</div><div>1</div><div>0</div><div>0</div><div>0</div><div>1</div><div>0</div><div>0</div><div>1</div></div></div></div>															
<div><div><div>Example 1: When M0 changes from 0→1, it will perform the 16-bit code conversion</div><div><div><div>M0</div><div><div>•</div><div>— </div><div>— </div><div>—EN</div></div></div><div><div>56P.G→B</div><div><div>S : D0</div><div>D : D100</div></div></div></div><div><div>Converting the 16-bit Gray-code in D0 into Binary-code, and then storing the result into D100.</div></div></div></div>															
<div><div>D0 = 1001010101010011B ➔ D100 = 1110011001100010B</div></div>															

FUN56   G→B	GRAY-CODE TO BINARY-CODE CONVERSION	FUN56   G→B
<p>Example 2: When M0 =1, it will perform the 32-bit code conversion</p> <div><div><div>M0</div><div>• </div><div>EN</div></div><div><div>56DP.G→B</div><div>S : D0</div><div>D : D100</div></div></div> <p>Converting the 32-bit Gray-code in DD0 into Binary-code, and then storing the result into DD100.</p> <p>DD0 = 00110111001001000010111100010100B → DD100 = 00100101110001111100101000011000B</p>		

Code Conversion Instructions

FUN 57 P DECOD	<div> <div>DECODE</div> </div>	FUN 57 P DECOD
--------------------------	--------------------------------	--------------------------

Ladder symbol

Decode control — EN

57P.DECOD

S :

Ns :

N_L :

D :

ERR — Range error

S : Source data register to be decoded (16 bits)

N_S : Starting bits to be decoded within S

N_L : Length of decoded value (1~8 bits)

D : Starting register storing decoded results (2~256 points = 1~16 words)

S, N_S, N_L, D may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number	V · Z P0~P9
S	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		<input type="checkbox"/>
N _S	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	0~15	<input type="checkbox"/>
N _L	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	2~256	<input type="checkbox"/>
D		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>		<input type="checkbox"/>

- This instruction, will set a single bit among the total of 2^{N_L} discrete points (D) to 1 and the others bit are set to 0. The bit number to be set to 1 is specified by the value comprised by BN_S~BN_S+N_L-1 of S (which is called the decode value, BN_S is the starting bit of the decode value, and BN_S+N_L-1 is the end value) .
- When decode control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), will take out the value BN_S~BN_S+N_L-1 from S. And with this value to locate the bit position and set D accordingly, and set all the other bit to zero
- This instruction only provides 16 bit operand, which means S only has B0~B15. Therefore the effective range of N_S is 0~15, and the N_L length of the decode value is limited to 1~8 bits. Therefore the width of the decoded result D is 2^{1~8} points = 2~256 points = 1~16 words (if 16 points are not sufficient, 1 word is still occupied). If the value of N_S or N_L is beyond the above range, will set the range-error flag "ERR" to 1, and do not carry out this instruction.
- If the end bit value exceeds the B15 of S, then will extend toward B0 of S + 1. However if this occurs then S+1 can't exceed the range of specific type of operand (ie. If S is of D type register then S+1 can't be D3072). If violate this, then this instruction only takes out the bits from starting bit BN_S to its highest limit as the decode value.

X0

EN

57P.DECOD

S : WX 0

Ns: 3

N_L: 5

D : R 2

ERR-

- The instruction at left takes out the data of five successive bits from X3 to X7 within the WX0 register and decodes it. The results are then stored in the 32-bit register starting at R2.

X15

X7

X3

X0

S

0

0

1

1

0

0

0

0

0

0

1

1

0

0

1

1

1

0

Length of decode value N_L=5,so bit value is formed by X7~X3 (equal 9)

↓ X0=

↑

R3

R2

D

0

0

0

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FUN 58 **P**
ENCOD


ENCODE


FUN 58 **P**
ENCOD


Ladder symbol


58P.ENCOD

Encode control — EN :  D=0 — All is 0

High/Low priority — H/L :  ERR — Range error

Ns : 

N_L : 

D : 

S : Starting register to be encoded

N_s : Bit position within S as the encoding start point

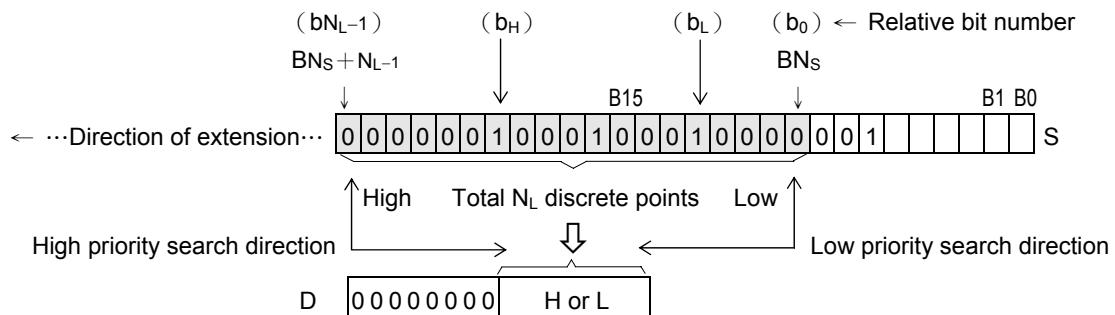
N_L : Number of encoding discrete points (2~256)

D : Number of register storing encoding results (1 word)

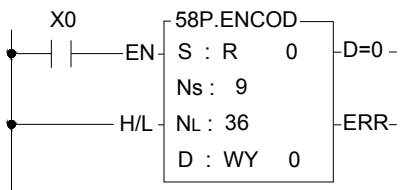
S, N_s, N_L, D may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	16-bit +/- number	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9
Oper- and														
S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>
N _s	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	0~15	<input type="radio"/>
N _L	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	2~256	<input type="radio"/>
D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>

- When encode control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), will starting from the points specified by N_s within S, take out towards the left (high position direction) N_L number of successive bits BN_s~BN_s+N_L-1 (BN_s is called the encoding start point, and its relative bit number is b₀;BN_s+N_L-1 is called the encoding end point, and its relative bit number is b_{N_L}-1). From left to right do higher priority (when H/L=1) encoding or from right to left do lower priority (when H/L=0) encoding (i.e. seek the first bit with the value of 1, and the relative bit number of this point will be stored into the low byte (B0~B7) of encoded resultant register D, and the high byte of D will be filled with 0.

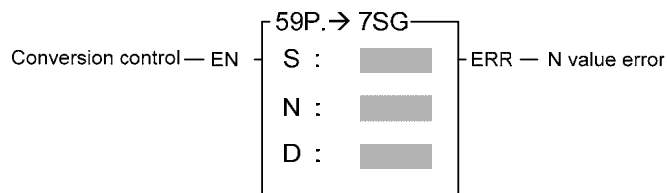


- As shown in the diagram above, for high priority encoding, the bit first to find is b_H (with a value of 12), and for low priority encoding, the bit first to find b_L (with a value of 4). Among the N_L discrete points there must be at least one bit with value of 1. If all bits are 0, will not to carry out this instruction, and the all zero flag "D=0" will set to 1.
- Because S is a 16-bit register, N_s can be 0~15, and is used to assign a point of B0~B15 within S as the encoding start point (b₀). The value of N_L can be 2~256, and it is used to identify the encoding end point, i.e. it assigns N_L successive single points starting from the start point (b₀) towards the left (high position direction) as the encoding zone (i.e. b₀~b_{N_L}-1). If the value of N_s or N_L exceeds the above value, then do not carry out this instruction, and set the range-error flag "ERR" as 1.

FUN 58 ENCOD	ENCODE	FUN 58 ENCOD																																																																																																																																																																			
<ul style="list-style-type: none">● If the encoding end point (bN_{L-1}) beyond the B15 of S, then continue extending towards S+1, S+2, but it must not exceed the range of specific type of operand. If it goes beyond this, then this instruction can only take the discrete points between b0 and the highest limit into account for encoding.																																																																																																																																																																					
<div style="display: flex; justify-content: space-between; align-items: flex-start;"><div style="width: 30%;"></div><div style="width: 65%;"><ul style="list-style-type: none">● The instruction at left is a high priority encode example. When X0 goes from 0 to 1, will take out toward left 36 successive bits starting from B9 (b0) specified by Ns within S, and perform high priority encoding (because H/L = 1). That is, starting from b35 (encoding end point), move right to find the first bit with the value of 1. The resultant value of this example is b26, so the value of D is 001AH=26, as shown in the diagram below.</div></div>																																																																																																																																																																					
<div style="display: flex; justify-content: space-around; align-items: flex-start;"><div style="width: 45%; text-align: center;"><p>S</p><table border="1" style="margin: auto;"><tr><td></td><td colspan="16" style="text-align: center;">(b0) B9</td><td></td></tr><tr><td></td><td>B15</td><td colspan="16"></td><td>B0</td></tr><tr><td>R0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>R1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>R2</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td></td><td>B47</td><td colspan="14"></td><td>B32</td></tr></table><p style="margin-top: 10px;">(b35) → (b26)</p><p style="margin-top: 10px;">The first bit with the value of 1 for high priority encoding</p></div><div style="width: 50%; text-align: center;"><p>D</p><table border="1" style="margin: auto;"><tr><td></td><td colspan="16" style="text-align: center;">Y15</td><td></td></tr><tr><td></td><td>Y0</td><td colspan="16"></td><td>Y15</td></tr><tr><td>WY0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr></table><p style="margin-top: 10px;">High byte always fill with "0" = 26 (encode value)</p></div></div>				(b0) B9																		B15																	B0	R0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0		B47															B32		Y15																		Y0																	Y15	WY0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
	(b0) B9																																																																																																																																																																				
	B15																	B0																																																																																																																																																			
R0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																																																																																																																																																				
R1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																																																																																																																																																				
R2	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0																																																																																																																																																				
	B47															B32																																																																																																																																																					
	Y15																																																																																																																																																																				
	Y0																	Y15																																																																																																																																																			
WY0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1																																																																																																																																																				

FUN 59 **P**
→7SG

7-SEGMENT CONVERSION

FUN 59 **P**
→7SGLadder symbol

S : Source data to be converted



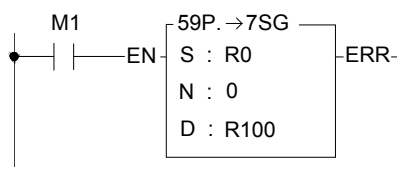
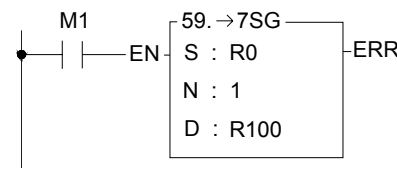
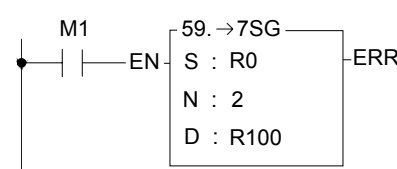
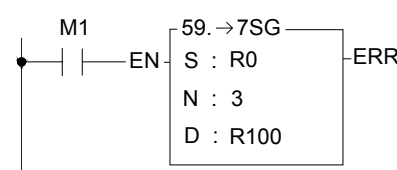
N : The nibble number within S for conversion

D : Register storing 7-segment result

S, N, D may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	16-bit +/- number	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9
S	○	○	○	○	○	○	○	○	○	○	○	○	○	○
N	○	○	○	○	○	○	○	○	○	○	○	○	0~3	○
D		○	○	○	○	○	○		○	○*	○*	○		○

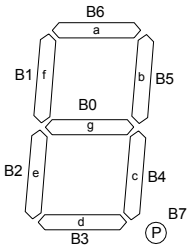
















- When conversion control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), will convert N+1 number of nibbles (A nibble is comprised by 4 successive bits, so B0~B3 of S form nibble 0, B4~B7 form nibble 1, etc...) within S to 7-segment code, and store the code into a low byte of D (High bytes does not change). The 7 segment within D are put in sequence, with "a" segment placed at B6, "b" segment at B5,, "g" segment at B0. B7 is not used and is fixed as 0. For details please refer the "7-segment code and display pattern table".
- Because this instruction is limited to 16 bits, and S only has 4 nibbles (NB0~NB3), the effective range of N is 0~3. Beyond this range, will set the N value flag error "ERR" to 1, and does not carry out this instruction.
- Care should be taken on total nibbles to be converted is N+1. N=0 means one digit to convert, N=1 means two digits to convert etc...
- When using the FATEK 7-segment expansion module(FBs-7SGxx) and the FUN84 (7SEG) handy instruction for mixing decoding and non-decoding application, FUN59 and FUN84 can be combined to simplify the program design.

FUN 59  →7SG	7-SEGMENT CONVERSION	FUN 59  →7SG
<p>〈 Example 1 〉 When M1 OFF→ON, convert hexadecimal to 7-Segment</p> <div></div> <p>R0=0001H Original R100=0000H ➔ R100=0030H (1)</p>		
<p>〈 Example 2 〉 When M1 ON, convert the hexadecimal to 7-Segment</p> <div></div> <p>R0=0056H ➔ R100=5B5FH (56)</p>		
<p>〈 Example 3 〉 When M1 ON, converting hexadecimal to 7-Segment</p> <div></div> <p>R0=0A48H Original R101=0000H ➔ R100=337FH (48) R101=0077H (A)</p>		
<p>〈 Example 4 〉 When M1 ON, convert hexadecimal to 7-Segment</p> <div></div> <p>R0=2790H ➔ R100=7B7EH (90) R101=6D72H (27)</p>		

FUN 59 **P**
→7SG

7-SEGMENT CONVERSION

FUN 59 **P**
→7SG

Nibble data of S		7-segment display format	Low byte of D								Display pattern
Hexadecimal number	Binary number		B7 ●	B6 a	B5 b	B4 c	B3 d	B2 e	B1 f	B0 g	
0	0000		0	1	1	1	1	1	1	0	
1	0001		0	0	1	1	0	0	0	0	
2	0010		0	1	1	0	1	1	0	1	
3	0011		0	1	1	1	1	0	0	1	
4	0100		0	0	1	1	0	0	1	1	
5	0101		0	1	0	1	1	0	1	1	
6	0110		0	1	0	1	1	1	1	1	
7	0111		0	1	1	1	0	0	1	0	
8	1000		0	1	1	1	1	1	1	1	
9	1001		0	1	1	1	1	0	1	1	
A	1010		0	1	1	1	0	1	1	1	
B	1011		0	0	0	1	1	1	1	1	
C	1100		0	1	0	0	1	1	1	0	
D	1101		0	0	1	1	1	1	0	1	
E	1110		0	1	0	0	1	1	1	1	
F	1111		0	1	0	0	0	1	1	1	

7-segment display pattern table

Code Conversion Instructions

FUN 60 P
 →ASC

ASCII CONVERSION

FUN 60 P
 →ASC

Ladder symbol

60P.→ASC

Conversion control — EN

S :

D :

S : Alphanumerics to be converted into ASCII code

D : Starting register storing ASCII results

Range	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	Alphanumeric
Ope- rand	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	1~12 alphanumeric
S											○
D	○	○	○	○	○	○	○	○*	○*	○	

- When conversion control "EN" = 1 or has a transition from 0 to 1 (P instruction), will convert alphabets and numbers stored in S (S has a maximum of 12 alphanumeric character) into ASCII and store it into registers starting from D. Each 2 alphanumeric characters occupy one 16-bit register.
- The application of this instruction, most often, stores alphanumeric information within a program, and waits until certain conditions occur, then converts this alphanumeric information into ASCII and conveys it to external display devices which can accept ASCII code.

- The instruction at left converts the 6 alphabets -ABCDEF into ASCII then stores it into 3 successive registers starting from R0.

S

Alphabet
ABCDEF

X0 =

⇒

D

	High Byte	Low Byte
R0	42 (B)	41 (A)
R1	44 (D)	43 (C)
R2	46 (F)	45 (E)

7-53

FUN 61 P
 →SEC

HOURL:MINUTE:SECOND TO SECONDS CONVERSION

FUN 61 P
 →SEC

Ladder symbol

61P.→SEC

Conversion control — EN

S :
 D :

D=0 — Result as 0

S : Starting calendar data register to be converted

D : Starting register storing results

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	—117968399
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	117964799
S	○	○	○	○	○	○	○	○	○	○	○	○	○
D		○	○	○	○	○	○		○	○*	○*	○	

- When conversion control "EN" = 1 or has a transition from 0 to 1 (P instruction), will convert the hour: minute: second data of S~S+2 into an equivalent value in seconds and store it into the 32-bit register formed by combining D and D+1. If the result = 0, then set the "D = 0" flag as 1.
- Among the FBs-PLC instructions, the hour: minute: second time related instructions (FUN61 and 62) use 3 words of register to store the time data, as shown in the diagram below. The first word is the second register, the second word is the minute register, and finally the third word is the hour register, and in the 16 bits of each register, only B14~B0 are used to represent the time value. While bit B15 is used to express whether the time values are positive or negative. When B15 is 0, it represents a positive time value, and when B15 is 1 it represents a negative time value. The B14~B0 time value is represented in binary, and when the time value is negative, B14~B0 is represented with the 2's complement. The number of seconds that results from this operation is the result of summation of seconds from the three registers representing hours: minutes: seconds.

S (sec)	B15	B14
S+1 (min)	—32768 sec~32767 sec	
S+2 (hr)	—32768 min~32767 min	
	—32768 hr~32767 hr	

↑
The B15 of each registers is used to represent the sign of each time value

⇒

D	B0	B15B0
D+1	the sec. value.	
	B31	B16

↑
B31 is used to represent the positive or negative nature of the sec. value

- Besides FUN61 or 62 instruction which treat hour: minute: second registers as an integral data, other instructions treat it as individual registers.
- The example program at below converts the hour: minute: second data formed by R20~R22 into their equivalent value in seconds then stored in the 32-bit register formed by R50~R51. The results are shown below.

S {	R20	0E11H	= 3601 sec
	R21	FD2FH	= - 721 min
	R22	03F3H	= 1011 hr

⇓ X0 = ⇓

D {	R50	EE45H	} = 3599941 sec
	R51	0036H	

7-54

Code Conversion Instructions

FUN 62 P →HMS	SECOND→HOUR : MINUTE : SECOND	FUN 62 P →HMS
---	--------------------------------------	---

Ladder symbol

Conversion control — EN —

62P.→HMS
 S :
 D :

D=0 — Result as 0

 OVR — Over range

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K
	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	-117968399
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	117964799
S	○	○	○	○	○	○	○	○	○	○	○	○	○
D		○	○	○	○	○	○		○	○*	○*	○	

- When conversion control "EN" = 1 or has a transition from 0 to 1 (P instruction), will convert the second data from the S~S+1 32-bit register into the equivalent hour : minute : second time value and store it in the three successive registers D~D+2. All the data in this instruction is represented in binary (if there is a negative value it is represented using the 2's complement.)

The bit B31 of the second register is used as the sign bit of the second value.

The bits B15 of each register are used as the sign bit of the hour : minute : second value.

- As shown in the diagram above, after convert to hour : minute : second value, the minute : second value can only be in the range of -59 to 59, and the hour number can be in the range of -32768 to 32767 hours. Because of this, the maximum limit of D is -32768 hours, -59 minutes, -59 seconds to 32767 hours, 59 minutes, 59 seconds, the corresponding second value of S which is in the range of -117968399 to 117964799 seconds. If the S value exceeds this range, this instruction cannot be carried out, and will set the over range flag "OVR" to 1. If S = 0 then result is 0 flag "D = 0" will be set to 1.
- The program in the diagram below is an example of this instruction. Please note that the content of the registers are denoted by hexadecimal, and on the right is its equivalent value in decimal notation.

R0	5D17H	}	6315287 sec
R1	0060H		

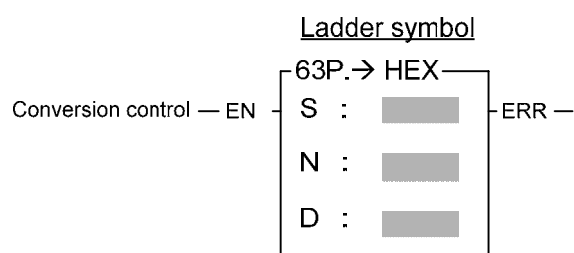
⇓ X0 = ⇓

R10	002FH	47 sec
R11	000EH	14 min
R12	06DAH	1754 hr

7-55

FUN 63 **P**
→HEX

CONVERSION OF ASCII CODE TO HEXADECIMAL VALUE

FUN 63 **P**
→HEX

S : Starting source register.



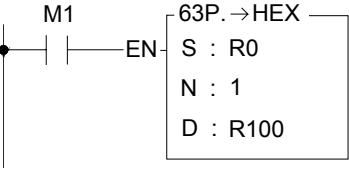
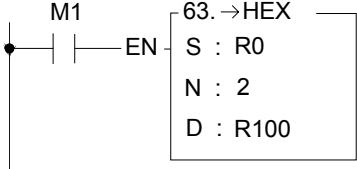
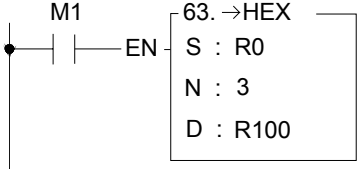
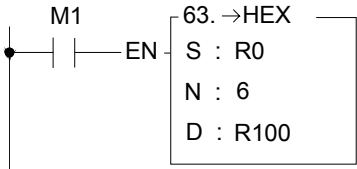
N : Number of ASCII codes to be converted to hexadecimal values.

D : The starting register that stores the result (hexadecimal value).

S, N, D, can associate with V, Z, P0~P9 to do the indirect addressing application.

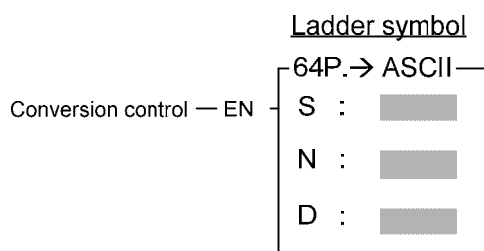
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16-bit +number	V ~ Z P0~P9
S	○	○	○	○	○	○	○	○	○	○	○	○		○
N	○	○	○	○	○	○	○	○	○	○	○	○	1~511	○
D		○	○	○	○	○	○		○	○*	○*	○		○

- When conversion control “EN” =1 or changes from 0→1(**P** instruction), it will convert the N successive hexadecimal ASCII character(‘0’~‘9’,‘A’~‘F’) convey by 16 bit registers (Low Byte is effective) into hexadecimal value, and store the result into the register starting with D. Every 4 ASCII code is stored in one register. The nibbles of register, which does not involve in the conversion of ASCII code will remain unchanged.
- The conversion will not be performed when N is 0 or greater than 511.
- When there is ASCII error (neither 30H~39H nor 41H~46H), the output “ERR” is ON.
- The main purpose of this instruction is to convert the hexadecimal ASCII character (‘0’~‘9’,‘A’~‘F’), which is received by communication port1 or communication port2 from the external ASCII peripherals, to the hexadecimal values that the CPU can process directly.

FUN 63  →HEX	CONVERSION OF ASCII CODE TO HEXADECIMAL VALUE	FUN 63  →HEX
<p>〈 Example 1 〉 When M1 from OFF→ON, ASCII code converted to hexadecimal value.</p> <div>  </div> <div> <ul style="list-style-type: none"> Converts the ASCII code of R0 into hexadecimal value and store to nibble0 (nibble1~nibble3 remain unchanged) of R100 </div> <div> <p>Originally R100=0000H R0=0039H (9) → R100=0009H</p> </div>		
<p>〈 Example 2 〉 When M1 is ON, ASCII code converted to hexadecimal value.</p> <div>  </div> <div> <ul style="list-style-type: none"> Converts the ASCII code of R0 and R1 into hexadecimal value and store to low byte (high byte remain unchanged) of R100 </div> <div> <p>Originally R100=0000H R0=0039H (9) R1=0041H (A) → R100=009AH</p> </div>		
<p>〈 Example 3 〉 When M1 is ON, ASCII code converted to hexadecimal value.</p> <div>  </div> <div> <ul style="list-style-type: none"> Converts the ASCII code of R0 and R1 into hexadecimal value and store result into R100 (nibble 3 remain unchanged) </div> <div> <p>Originally R100=0000H R0=0039H (9) R1=0041H (A) R2=0045H (E) → R100=009AEH</p> </div>		
<p>〈 Example 4 〉 When M1 is ON, ASCII code converted to hexadecimal value.</p> <div>  </div> <div> <ul style="list-style-type: none"> Converts the ASCII code of R0~R5 into hexadecimal value and store it to R100~R101 </div> <div> <p>Originally R100=0000H R101=0000H R0=0031H (1) R1=0032H (2) R2=0033H (3) R3=0034H (4) R4=0035H (5) → R100=3456H R5=0036H (6) R101=0012H</p> </div>		

FUN 64 **P**
→ASCII



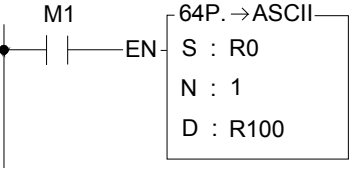
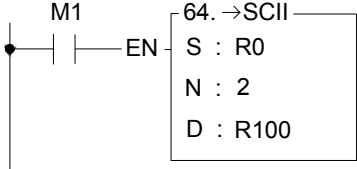
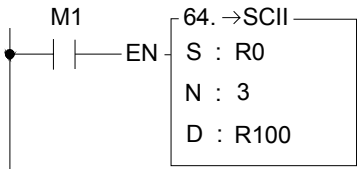
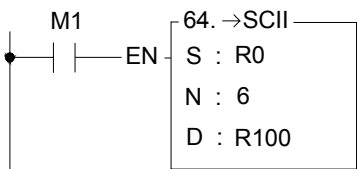
CONVERSION OF HEXADECIMAL VALUE TO ASCII CODE

FUN 64 **P**
→ASCII

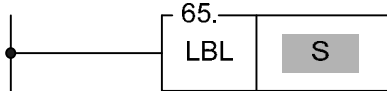
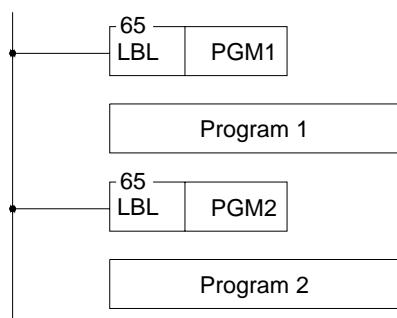
S : Starting source register
 N : Number of hexadecimal digit to be converted to ASCII code.
 D : The starting register storing result.
 S, N, D, can associate with V, Z, P0~P9 to do the indirect addressing application.




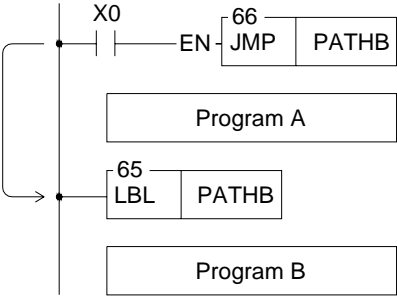
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16-bit + number	V ~ Z P0~P9
S	○	○	○	○	○	○	○	○	○	○	○	○		○
N	○	○	○	○	○	○	○	○	○	○	○	○	1~511	○
D		○	○	○	○	○	○		○	○*	○*	○		○




- When conversion control "EN" =1 or changes from 0→1(**P** instruction), will convert the N successive nibbles of hexadecimal value in registers start from S into ASCII code, and store the result to low byte (high byte remain unchanged) of the registers which start from D.
- The conversion will not be performed when the value of N is 0 or greater than 511.
- The main purpose of this instruction is to convert the numerical value data, which PLC has processed, to ASCII code and transmit to ASCII peripherals by communication port1 or communication port 4.

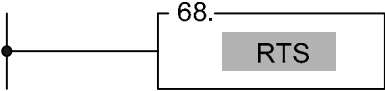
FUN 64  →ASCII	CONVERSION OF HEXADECIMAL VALUE TO ASCII CODE	FUN 64  →ASCII
<p>〈 Example 1 〉 When M1 changes from OFF→ON, it converts hexadecimal value to ASCII code.</p>		
		
<p>R0=0009H ➔ R100=0039H (9)</p>	<ul style="list-style-type: none"> • Converts the Nibble 0 of R0 to ASCII code and stores it into R100 (High byte does not change). 	
<p>〈 Example 2 〉 When M1 is ON, it converts hexadecimal value to ASCII code.</p>		
		
<p>R0=009AH ➔ R100=0039H (9) R101=0041H (A)</p>	<ul style="list-style-type: none"> • Converts the NB0~NB1 of R0 to ASCII code and stores it into R100 ~ R101 (high bytes remain unchanged). 	
<p>〈 Example 3 〉 When M1 is ON, it converts hexadecimal value to ASCII code.</p>		
		
<p>R0=0123H ➔ R100=0031H (1) R101=0032H (2) R102=0033H (3)</p>	<ul style="list-style-type: none"> • Converts the NB0~NB2 of R0 to ASCII code and stores it into R100~R102 	
<p>〈 Example 4 〉 When M1 is ON, it converts hexadecimal value to ASCII code.</p>		
		
<p>R0=3456H ➔ R100=0031H (1) R1=0012H R101=0032H (2) R102=0033H (3) R103=0034H (4) R104=0035H (5) R105=0036H (6)</p>	<ul style="list-style-type: none"> • Converts the NB0~NB5 of R0~R1 to ASCII code and stores it into R100~R105 	

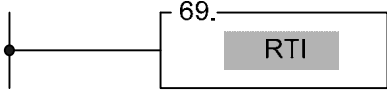
END	PROGRAM END	END
<p style="text-align: center;"><u>Ladder symbol</u></p> <div style="display: flex; align-items: center; justify-content: space-around;"> <div style="text-align: center;"> End control — EN — <div style="border: 1px solid black; padding: 2px 10px; background-color: #cccccc; display: inline-block;">END</div> </div> <div>No operand</div> </div>		
<ul style="list-style-type: none"> When end control "EN" = 1, this instruction is activated. Upon executing the END instruction and "EN" = 1, the program flow will immediately returns to the starting point (0000M) to restart the next scan – i.e. all the programs after the END instruction will not be executed. When "EN" = 0, this instruction is ignored, and programs after the END instruction will continue to be executed as the END instruction is not exist. This instruction may be placed more than one point within a program, and its input (end control "EN") controls the end point of program execution. It is especially useful for debugging and for testing. It's not necessary to put any END instructions in the main program, CPU will automatic restart to start point when reach the end of main program. <div style="margin-top: 20px;"> </div>		

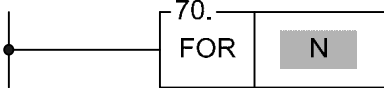
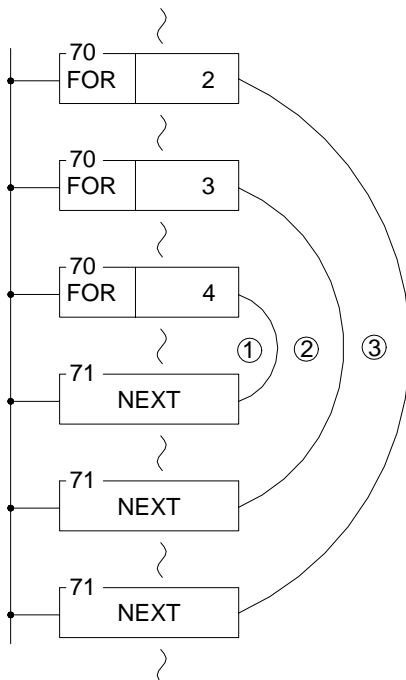
FUN 65 LBL	LABEL	FUN 65 LBL												
<div> <div> <div>Ladder symbol</div> <div>  </div> </div> <div>S : Alphanumeric, 1~6 characters</div> </div>														
<div> <ul style="list-style-type: none"> ● This instruction is used to make a tag on certain address within a program, to provide a target address for execution of JUMP, CALL instruction and interrupt service. It also can be used for document purpose to improve the readability and interpretability of the program. ● This instruction serves only as the program address marking to provide the control of procedure flow or for remark. The instruction itself will not perform any actions; whether the program contains this instruction or not, the result of program execution will not be influenced by this instruction. ● The label name can be formed by any 1~6 alphanumeric characters and can't be duplicate in the same program. The following label names are reserved for interrupt function usage. These "reserved words", can't be used for normal program labels. <table> <tr> <th>Reserved words</th> <th>Description</th> </tr> <tr> <td>X0+I~X15+I (INT0~INT15) X0-I~X15-I (INT0-~INT15-)</td> <td>labels for external input (X0~X15) interrupt service routine.</td> </tr> <tr> <td>HSC0I~HSC7I</td> <td>labels for high speed counter HSC0~HSC7 interrupt service routine.</td> </tr> <tr> <td>1MSI (1MS) 、2MSI (2MS) 、3MSI (3MS) 、 4MSI (4MS) 、5MSI (5MS) 、10MSI (10MS) 、 50MSI (50MS) 、100MSI (100MS)</td> <td>Labels for 8 kinds of internal timer interrupt service routine.</td> </tr> <tr> <td>HSTAI (ATMRI) 、HST0I~HST3I</td> <td>Label for High speed fixed timer interrupt service routine.</td> </tr> <tr> <td>PSO0I~PSO3I</td> <td>Labels for the pulse output command finished interrupt service routine.</td> </tr> </table> <p>Only the interrupt service routine can use the label names listed on above table, if mistaken on using the reserved label on the normal subroutine can cause the CPU fail or unpredictable operation.</p> <p>The label of following diagram illustration served only as program remarks (it is not treated as a label for call or jump target). For the application of labeling in jump control, please refer to JMP instruction for explanation. As to the labeling serves as subroutine names, please refer to CALL instruction for details.</p> <div>  </div> </div>			Reserved words	Description	X0+I~X15+I (INT0~INT15) X0-I~X15-I (INT0-~INT15-)	labels for external input (X0~X15) interrupt service routine.	HSC0I~HSC7I	labels for high speed counter HSC0~HSC7 interrupt service routine.	1MSI (1MS) 、2MSI (2MS) 、3MSI (3MS) 、 4MSI (4MS) 、5MSI (5MS) 、10MSI (10MS) 、 50MSI (50MS) 、100MSI (100MS)	Labels for 8 kinds of internal timer interrupt service routine.	HSTAI (ATMRI) 、HST0I~HST3I	Label for High speed fixed timer interrupt service routine.	PSO0I~PSO3I	Labels for the pulse output command finished interrupt service routine.
Reserved words	Description													
X0+I~X15+I (INT0~INT15) X0-I~X15-I (INT0-~INT15-)	labels for external input (X0~X15) interrupt service routine.													
HSC0I~HSC7I	labels for high speed counter HSC0~HSC7 interrupt service routine.													
1MSI (1MS) 、2MSI (2MS) 、3MSI (3MS) 、 4MSI (4MS) 、5MSI (5MS) 、10MSI (10MS) 、 50MSI (50MS) 、100MSI (100MS)	Labels for 8 kinds of internal timer interrupt service routine.													
HSTAI (ATMRI) 、HST0I~HST3I	Label for High speed fixed timer interrupt service routine.													
PSO0I~PSO3I	Labels for the pulse output command finished interrupt service routine.													

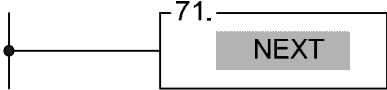
FUN 66  JMP	JUMP	FUN 66  JMP
<p style="text-align: center;"><u>Ladder symbol</u></p> <div style="display: flex; align-items: center; justify-content: space-between;"> <div style="text-align: center;"> <p>Jump control — EN</p> <div style="border: 1px solid black; padding: 5px; display: inline-block;"> <div style="border-bottom: 1px solid black; padding-bottom: 2px;">66P.</div> <div style="display: flex; justify-content: space-between; padding: 2px;"> JMP LBL </div> </div> </div> <div style="text-align: center;"> <p>LBL : The program label to be jumped</p> </div> </div>		
<ul style="list-style-type: none"> When jump control “EN”=1 or changes from 0→1 ( instruction), PLC will jump to the location behind the marked label and continuous to execute the program. This instruction is especially suit for the applications where some part of the program will be executed only under certain condition. This can shorter the scan time while not executes the whole program. This instruction allows jump backward (i.e. the address of LBL is comes before the address of JMP instruction). However, care should be taken if the jump action cause the scan time exceed the limit set by the watchdog timer, the WDT interrupt will be occurred and stop executing. The jump instruction allows only for jumping among main program or jumping among subroutine area, it can't jump across main/subroutine area. <div style="display: flex; align-items: flex-start; margin-top: 20px;"> <div style="flex: 1;">  </div> <div style="flex: 1; padding-left: 20px;"> <ul style="list-style-type: none"> In the left diagram, when X0=1, the program will jump directly to the LBL position named PATHB and continuing to execute program B. Therefore it will skip the program A and none of the instructions of program A will be executed. The status of registers and the coils associated with program A will keep unchanged (as if there is no program section A). </div> </div>		

FUN 67  CALL	CALL	FUN 67  CALL
<p style="text-align: center;"><u>Ladder symbol</u></p> <div><div>Call control — EN</div><div><div>67P.</div><div>CALL</div><div>LBL</div></div></div> <p style="text-align: right;">LBL : The subroutine label name to be called.</p>		
<div><div><ul style="list-style-type: none">When call control “EN”=1 or changes from 0→1 ( instruction), PLC will call (perform) the subroutine bear the same label name as the one being called. When execute the subroutine, the program will execute continuous as normal program does but when the program encounter the RTS instruction then the flow of the program will return back to the address immediately after the CALL instruction.All the subroutines must end with one “return from subroutine instruction RTS” instruction; otherwise it will cause executing error or CPU shut down. Nevertheless, an RTS instruction can be shared by subroutines (so called as multiple entering subroutines; even though the entry points are different, they have a same returning path) as illustrated in the right diagram subroutine SUB1~3.When main program called a subroutine, the subroutine also can call the other subroutines (so called the nested subroutines) for up to 5 levels at the most (include the interrupt routine).</div><div><div><div><div>1X</div><div>CALL SUB1</div></div><div>2X</div><div><div>LBL SUB1</div><div>CALL SUB2</div><div>RTS</div></div><div>3X</div><div><div>LBL SUB2</div><div>CALL SUB3</div><div>RTS</div></div><div>4X</div><div><div>LBL SUB3</div><div>CALL SUB4</div><div>RTS</div></div><div>5X</div><div><div>LBL SUB4</div><div>RTS</div></div></div><div><div>Main program area</div><div>Subroutine area</div></div></div><div><div><div><div>65</div><div>LBL</div><div>SUB1</div></div><div>Program 1</div><div><div>66</div><div>JMP</div><div>SUB3</div></div><div>65</div><div>LBL</div><div>SUB2</div><div>Program 2</div><div><div>65</div><div>LBL</div><div>SUB3</div></div><div>Program 3</div><div><div>68</div><div>RTS</div></div></div><div><div>SUB1</div><div>SUB2</div><div>SUB3</div></div></div><div><ul style="list-style-type: none">Interrupt service programs (HSC0I~HSC7I、PSO0I~PSO3I、X0+I~X15+I/INT0~INT15、X0-I~X15-I/INT0-~INT15-、HSTAI/ATMRI、1MSI/1MS、2MSI/2MS、3MSI/3MS、4MSI/4MS、5MSI/5MS、10MSI/10MS、50MSI/50MS、100MSI/100MS) are also a kind of subroutine. It is also placed in sub program area. However, the calling of interrupt service program is triggered off by the signaling of hardware to make the CPU perform the corresponding interrupt service program (which we called as the calling of the interrupt service program). The interrupt service program can also call subroutine or interrupted by other interrupts with higher priority. Since it is also a subroutine (which occupied one level), it can only call or interrupted by 4 levels of subroutine or interrupt service program. Please refer to RTI instruction for explanation.</div></div>		

FUN 68 RTS	RETURN FROM SUBROUTINE	FUN 68 RTS
<p style="text-align: center;"><u>Ladder symbol</u></p> 		
<ul style="list-style-type: none"> ● This instruction is used to represent the end of a subroutine. Therefore it can only appear within the subroutine area. Its input side has no control signal, so there is no way to serially connect any contacts. This instruction is self sustain, and is directly connected to the power line. ● When PLC encounter this instruction, it means that the execution of a subroutine is finished. Therefore it will return to the address immediately after the CALL instruction, which were previously executed and will continue to execute the program. ● If this instruction encounters any of the three flow control instructions MC, SKP, or JMP, then this instruction may not be executed (it will be regarded as not exist). If the above instructions are used in the subroutine and causing the subroutine not to execute the RTS instruction, then PLC will halt the operation and set the M1933(flow error flag) to 1. Therefore, no matter what the flow is going, it must always ensure that any subroutine must be able to execute a matched RTS instruction. ● For the usage of the RTS instruction please refer to instructions for the CALL instruction. 		

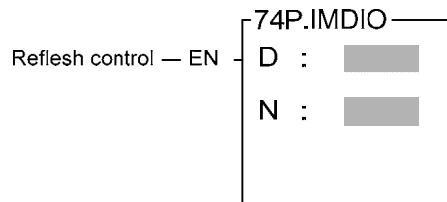
FUN 69 RTI	RETURN FROM INTERRUPT	FUN 69 RTI
<p style="text-align: center;"><u>Ladder symbol</u></p> 		
<ul style="list-style-type: none"> ● The function of this instruction is similar to RTS. Nevertheless, RTS is used to end the execution of sub program, and RTI is used to end the execution of interrupt service program. Please refer to the explanation of RTS instruction. ● A RTI instruction can be shared by more than one interrupt service program. The usage is the same as the sharing of an RTS by many subroutines. Please refer to the explanation of CALL instruction. ● The difference between interrupts and call is that the sub program name (LBL) of a call is defined by user, and the label name and its call instruction are included in the main program or other sub program. Therefore, when PLC performs the CALL instruction and the input “EN”=1 or changes from 0→1 (P instruction), the PLC will call (execute) this sub program. For the execution of interrupt service program, it is directly used with hardware signals to interrupt CPU to pause the other less important works, and then to perform the interrupt service program corresponding to the hardware signal (we call it the calling of interrupt service program). In comparing to the call instruction that need to be scanned to execute, the interrupt is a more real time in response to the event of the outside world. In addition, the interrupt service program cannot be called by label name; therefore we preserve the special “reserved words” label name to correspond to the various interrupts offered by PLC (check FUN65 explanation for details). For example, the reserved word X0+I is assigned to the interrupt occurred at input point X0; as long as the sub program contains the label of X0+I, when input point X0 interrupt is occurred (X0: \uparrow), the PLC will pause the other lower priority program and jump to the subroutine address which labeled as X0+I to execute the program immediately. ● If there is a interrupt occurred while CPU is handling the higher priority (such as hardware high speed counter interrupt) or same priority interrupt program (please refer to Chapter 10 for priority levels), the PLC will not execute the interrupt program for this interrupt until all the higher priority programs were finished. ● If the RTI instruction cannot be reached and performed in the interrupt service routine, may cause a serious CPU shut down. Consequently, no matter how you control the flow of program, it must be assured that the RTI instruction will be executed in any interrupt service program. ● For the detailed explanation and example for the usage of interrupts, please refer to Chapter 9 for explanation. 		

FUN 70 FOR	FOR												FUN 70 FOR																																																																					
Ladder symbol																																																																																		
		N : Number of times of loop execution																																																																																
<table border="1"><thead><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th></tr></thead><tbody><tr><td rowspan="2">Ope- rand</td><td>WX0</td><td>WY0</td><td>WM0</td><td>WS0</td><td>T0</td><td>C0</td><td>R0</td><td>R3840</td><td>R3904</td><td>R3968</td><td>R5000</td><td>D0</td><td>1</td></tr><tr><td> </td><td> </td><td> </td><td> </td><td> </td><td> </td><td> </td><td> </td><td> </td><td> </td><td> </td><td> </td><td> </td></tr><tr><td></td><td>WX240</td><td>WY240</td><td>WM1896</td><td>WS984</td><td>T255</td><td>C255</td><td>R3839</td><td>R3903</td><td>R3967</td><td>R4167</td><td>R8071</td><td>D4095</td><td>16383</td></tr><tr><td>N</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td></tr></tbody></table>		Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	1															WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	16383	N	○	○	○	○	○	○	○	○	○	○	○	○	○												
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K																																																																					
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	1																																																																					
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	16383																																																																					
N	○	○	○	○	○	○	○	○	○	○	○	○	○																																																																					
<ul style="list-style-type: none">● This instruction has no input control, is connected directly to the power line, and cannot be in series with any conditions.● The programs within the FOR and NEXT instructions form a program loop (the start of the loop program is the next instruction after FOR, and the last is the instruction before NEXT). When PLC executes the FOR instruction, it first records the N value after that instruction (loop execution number), then for N times successively execution from start to last of the programs in the loop. Then it jumps out of the loop, and continues executes the instruction immediately after the NEXT instruction.● The loop can have a nested structure, i.e. the loop includes other loops, like an onion. 1 loop is called a level, and there can be a maximum of 5 levels. The FOR and NEXT instructions must be used in pairs. The first FOR instruction and the last NEXT instruction are the outermost (first) level of a nested loop. The second FOR instruction and the second last NEXT instruction are the second level, the last FOR instruction and the first NEXT instruction form the loop's innermost level.																																																																																		
		<ul style="list-style-type: none">● In the example in the diagram at left, loop ① will be executed $4 \times 3 \times 2 = 24$ times, loop ② will be executed $3 \times 2 = 6$ times, and loop ③ will be executed 2 times.● If there is a FOR instruction and no corresponding NEXT instruction, or the FOR and NEXT instructions in the nested loop have not been used in pairs, or the sequence of FOR and NEXT has been misplaced, then a syntax error will be generated and this program may not be executed.● In the loop, the JMP instruction may be used to jump out of the loop. However, care must be taken that once the loop has been entered (and executed to the FOR instruction), no matter how the program flow jumps, it must be able to reach the NEXT instruction before reaching the END instruction or the bottom of the program. Otherwise FBs-PLC will halt the operation and show an error message.● The effective range of N is 1~16383 times. Beyond this range FBs-PLC will treat it as 1. Care should be taken , if the amount of N is too large and the loop program is too big, a WDT may occur.																																																																																

FUN 71 NEXT	LOOP END	FUN 71 NEXT
<p><u>Ladder symbol</u></p> 		
<ul style="list-style-type: none">● This instruction and the FOR instruction together form a program loop. The instruction itself has no input control, is connected directly to the power line, and cannot be in series with any conditions.● When PLC has not yet entered the loop (has not yet executed to the FOR instruction, or has executed but then jumped out), but the NEXT instruction is reached, then PLC will not take any action, just as if this instruction did not exist.● For the usage of this instruction please refer to the explanations for the FOR instruction on the preceding page.		

FUN 74 **P**
IMDIO

IMMEDIATE I/O

FUN 74 **P**
IMDIOLadder symbol



D : Starting number of I/O points to be refreshed
 N : Number of I/O points to be refreshed

Range Ope- rand	X	Y	K
	Xn of Main Unit.	Yn of Main Unit.	1 36
D	○	○	
N			○

- For normal PLC scan cycle, the CPU gets the entire input signals before the program is executed, and then perform the executing of program based on the fresh input signals. After finished the program execution the CPU will update all the output signals according to the result of program execution. Only after the complete scan has been finished will all the output results be transferred all at once to the output. Thus for the input event to output responses, there will be a delay of at least 1 scan time (maximum of 2 scan time). With this instruction, the input signals or output signals specified by this instruction can be immediately refresh to get the faster input to output response without the limitation imposed by the scan method.
- When refresh control "EN" = 1 or has a transition from 1 to 0(**P** instruction), then the status of N input points or output points (D~D+N-1) will be refreshed.
- The I/O points for FBs-PLC's immediate I/O are only limited to I/O points on the main unit. The table below shows permissible I/O numbers for 20, 32, 40 and 60 point main units:

Main-unit type Permissible numbers	10 points	14 points	20 points	24 points	32 points	40 points	60 points
Input signals	X0~X5	X0~X7	X0~X11	X0~X13	X0~X19	X0~X23	X0~X35
Output signals	Y0~Y3	Y0~Y5	Y0~Y7	Y0~Y9	Y0~Y11	Y0~Y15	Y0~Y23


- If the intended refresh I/O signals of this instruction is beyond the range of I/O points specified on above table then PLC will be unable to operate and the M1931 error flag will be set to 1. (for example, if in a program, D=X11, N=10, which means X11 to X20 are to be immediately retrieved. Supposing the main unit is FBs-32MA, then its biggest input point is X19, and clearly X20 has already exceeded the main unit's input point number so under such case M1931 error flag will be set to 1).
- With this instruction, PLC can immediately refresh input/output signals. However, the delay of the hardware or the software filter impose on the I/O signals still exist. Please pay attention on this.


FUN 76 		DECIMAL- KEY INPUT										FUN 76 	
TKEY												TKEY	


Ladder symbol

Input control — EN

76D.TKEY

IN : 

D : 

KL : 















— KPR — Key in action

IN : Key input point

D : register storing key-in numerals

KL: starting coil to reflect the input status

D may combine with V, Z, P0~P9 to serve indirect address application

Range	X	Y	M	S	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	XR
Ope- rand	X0	Y0	M0	S0	WY0	WM0	WS0	T0	C0	R0	R3904	R3968	R5000	D0	V · Z
	X240	Y240	M1896	S984	WY240	WM1896	WS984	T255	C255	R3839	R3967	R4167	R8071	D4095	P0~P9
IN															
D															
KL															

- This instruction has designated 10 input points IN~IN+9 (IN0~IN9) to one decimal number entry (IN->0, IN+1->1...). According to the key-in sequence (ON) of these input points, it is possible to enter 4 or 8 decimal numbers into the registers specified by D.
- When input control "EN" = 1, this instruction will monitor the 10 input points starting from IN and put the corresponding number into D register while the key were depressed. It will wait until the input point has released, then monitor the next "ON" input point, and shift in the new number into D register (high digit is older than low digit) . For the 16-bit operand, D register can store up to 4 digits, and for the 32-bit operand 8 digits may be stored. When the key numbers full fill the D register, new key-in number will kick out the oldest key number of the D register. The key-in status of the 10 input points starting from IN will be recorded on the 10 corresponding coil starting from KL. These coils will set to 1 while the corresponding key is depressed and remain unchanged even if the corresponding key is released. Until other key is depressed then it will return to zero. As long as any input point is depressed (ON), then the key-in flag KPR will set to 1. Only one of IN0~IN9 key can be depressed at the same time. If more than one is pressed, then the first one is the only one taken. Below is a schematic diagram of the function with 16-bit operand.
- When input control "EN" = 0, this instruction will not be executed. KPR output and KL coil status will be 0. However, the numerical values of D register will remain unchanged.

Key-in
IN0 ~ IN9

0

1

2

.....

9

BCD Code

Forced out

1000S

100S

10S

1S

D

BIN(0~9999)

X20

EN

76.TKEY

IN : X 0


D : R 0

KL : M 0


KPR — ()

Y0

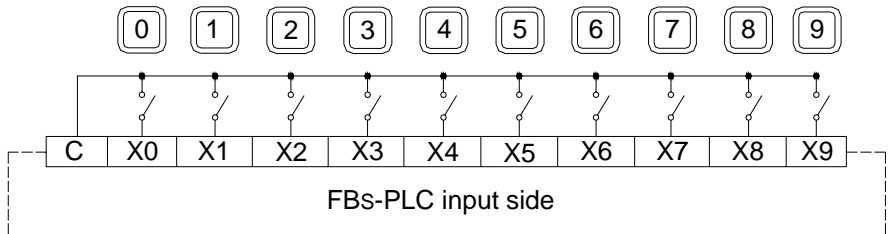
- The instruction at left represents the input point X0 with the number "0", X1 is represented by 1, ... , M0 records the action of X0, M1 records the action of X1 ... , and the input numerical values are stored in the R0 register.

FUN 76 
TKEY

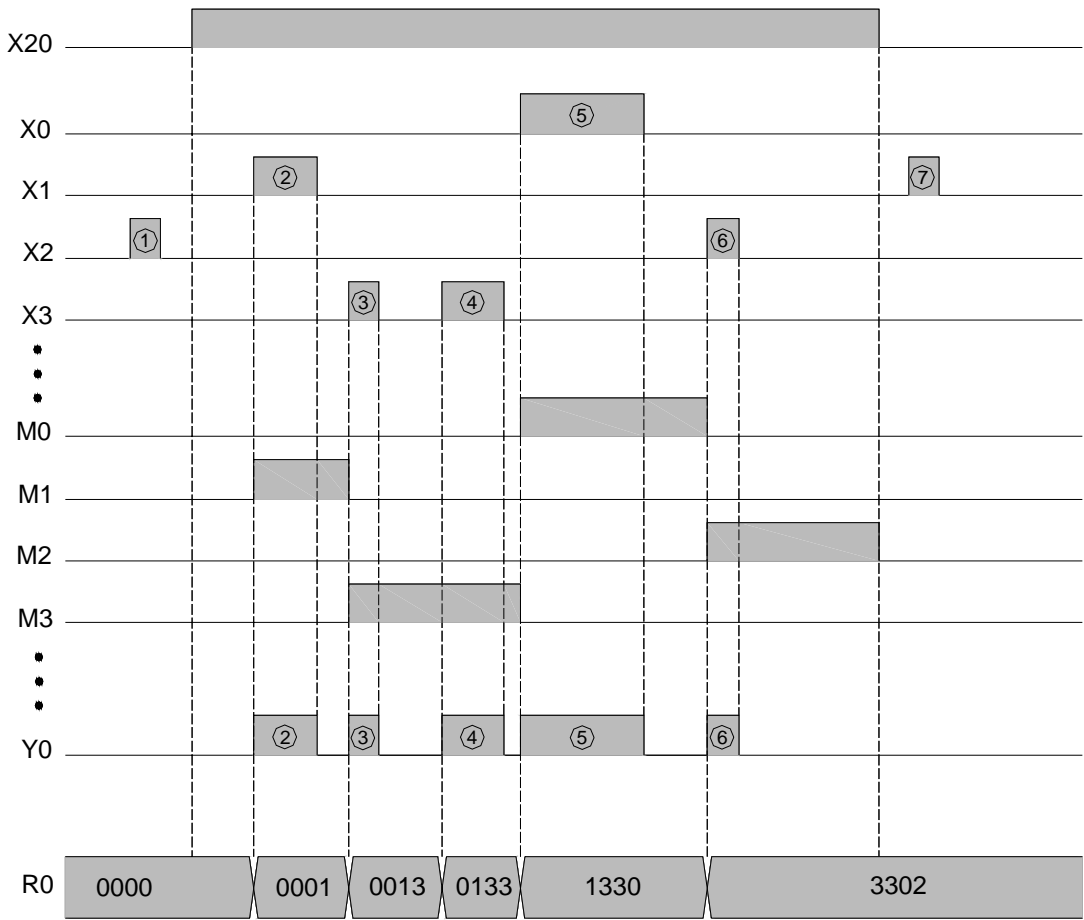
DECIMAL- KEY INPUT
























































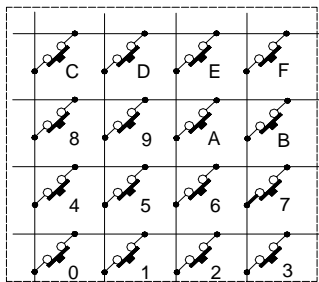
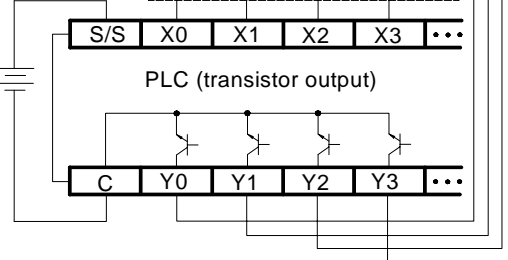
FUN 76 
TKEY


The following diagram is the input wiring schematic for this example:



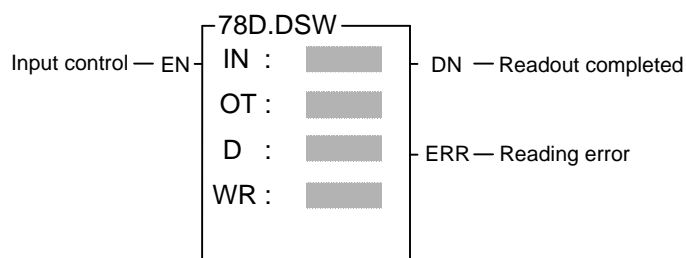
- If the X0~X3 key-in sequence follow the ① ② ③ ④ ⑤ ⑥ ⑦ sequence in the following diagram. At step ① and ⑦ the X20 is 0, so there was no key generated, only steps ② ③ ④ ⑤ ⑥ are effective. Because the register can only hold 4 key numbers, Of these 5 steps the first key was kick out. The key strokes 3302 of the steps ③ ④ ⑤ ⑥ are entered in the R0 register.



FUN 77  HKEY	HEX-KEY INPUT	FUN 77  HKEY																																																																																																															
<div><div><div><div>Ladder symbol</div><div><div>Execution control — EN</div><div><div>77D.HKEY</div><div><div>IN : </div><div>OT : </div><div>D : </div><div>KL : </div><div>WR : </div></div><div><div>NKP — Number key press</div><div>FKP — Function key press</div></div></div></div><div><div>IN : Starting of digital input for key scan</div><div>OT: Starting of digital output for multiplexing key scan (4 points)</div><div>D : Register to store key-in numbers</div><div>KL: Starting relay for key status</div><div>WR: Working register, it can't repeat in use</div><div>D may combine with V · Z · P0~P9 to serve indirect addressing application</div></div></div></div></div>																																																																																																																	
<table><tr><th>Range</th><th>X</th><th>Y</th><th>M</th><th>S</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>XR</th></tr><tr><td rowspan="2">Ope- rand</td><td>X0</td><td>Y0</td><td>M0</td><td>S0</td><td>WY0</td><td>WM0</td><td>WS0</td><td>T0</td><td>C0</td><td>R0</td><td>R3904</td><td>R3968</td><td>R5000</td><td>D0</td><td>V · Z</td></tr><tr><td>X240</td><td>Y240</td><td>M1896</td><td>S984</td><td>WY240</td><td>WM1896</td><td>WS984</td><td>T255</td><td>C255</td><td>R3839</td><td>R3967</td><td>R4167</td><td>R8071</td><td>D4095</td><td>P0~P9</td></tr><tr><td>IN</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>OT</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>D</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>KL</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table>			Range	X	Y	M	S	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	XR	Ope- rand	X0	Y0	M0	S0	WY0	WM0	WS0	T0	C0	R0	R3904	R3968	R5000	D0	V · Z	X240	Y240	M1896	S984	WY240	WM1896	WS984	T255	C255	R3839	R3967	R4167	R8071	D4095	P0~P9	IN																OT																D																KL															
Range	X	Y	M	S	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	XR																																																																																																		
Ope- rand	X0	Y0	M0	S0	WY0	WM0	WS0	T0	C0	R0	R3904	R3968	R5000	D0	V · Z																																																																																																		
	X240	Y240	M1896	S984	WY240	WM1896	WS984	T255	C255	R3839	R3967	R4167	R8071	D4095	P0~P9																																																																																																		
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D																																																																																																																	
KL																																																																																																																	
<div><div><div><div><div>●</div><div>The numeric (0~9) key function of this instruction is similar as for the TKEY instruction. The hardware connection for TKEY and HKEY is different. For TKEY instruction each key have one input point to connect, while HKEY use 4 input points and 4 output points to form a 4x4 multiplex 16 key input. 4x4 means that there can be 16 input keys, so in addition to the 10 numeric keys, the other 6 keys can be used as function keys (just like the usual discrete input). The actions of the numeric keys and the function keys are independent and have no effect on each other.</div></div></div><div><div><div><div>●</div><div>When execution control "EN" = 1, this instruction will scan the numeric keys and function keys in the matrix formed by the 4 input points starting from IN and the 4 output points starting from OT. For the function of the numeric keys and "NKP" output please refer to the TKEY instruction. The function keys maintain the key-in status of the A~F keys in the last 6 relays specified by KL (the first 10 store the key-in status of the numeric keys). If any one of the A~F keys is depressed, FKP (FO1) will set to 1. The OT output points for this instruction must be transistor outputs.</div></div></div><div><div><div><div>●</div><div>The biggest number for a 16-bit operand is 4 digits (9999), and for 32-bit operand is 8 digits (99999999). However, there are only 6 function keys (A~F), no matter whether it is a 16-bit or 32-bit operand.</div></div></div></div></div><div><div><div><div><div><div>X10</div><div>EN</div><div>77D.HKEY</div><div><div>IN : X0</div><div>OT : Y0</div><div>D : R0</div><div>KL : M0</div><div>WR : D0</div></div><div><div>NKP — () M10</div><div>FKP — () M11</div></div></div></div><div><div><div>Function Keys</div><div>Numeric Keys</div></div><div><div>24V</div><div>PLC (transistor output)</div></div></div></div><div><div><div><div>●</div><div>The instruction in the diagram above uses X0~X3 and Y0~Y3 to form a multiplex key input. It can input numeric values of 8 digits and stores the results in R1R0. The input status of the function keys is stored in M10(A~F).</div></div></div></div></div></div></div></div>																																																																																																																	

FUN 78 
DSW

DIGITAL SWITCH INPUT














FUN 78 
DSWLadder symbol

IN : Starting of input for thumb wheel switch

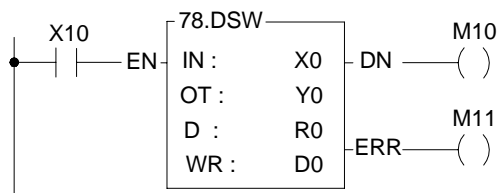
OT: Starting of output for multiplexing scan
(4 points)

D : Register to store readout value

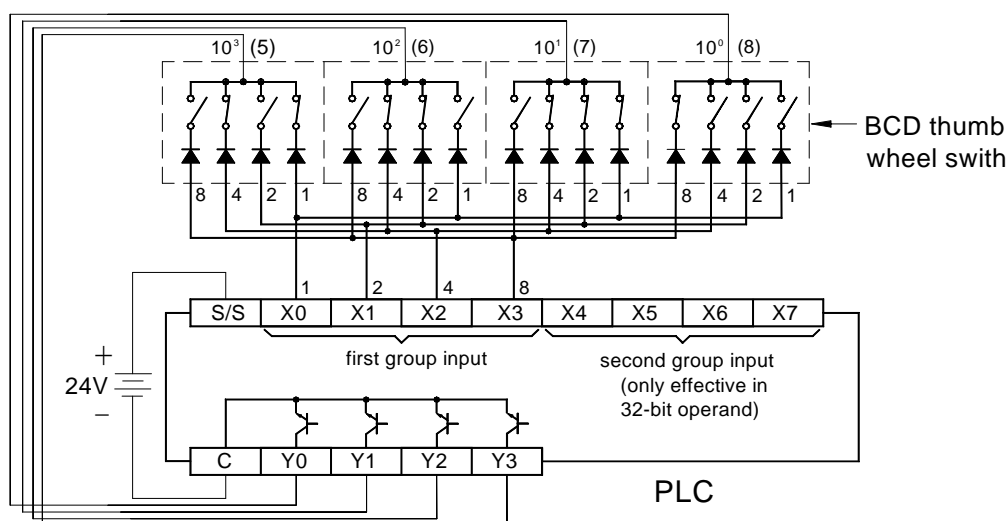
WR: Working register, it can't repeat in use
(WR & WR+1 for 16-bit operation;
WR, WR+1 & WR+2 for 32-bit operation)D may combine with V · Z · P0~P9 to serve
indirect addressing application

Range	X	Y	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	XR
	X0	Y0	WY0	WM0	WS0	T0	C0	R0	R3904	R3968	R5000	D0	V · Z
Oper- and	X240	Y240	WY240	WM1896	WS984	T255	C255	R3839	R3967	R4167	R8071	D4095	P0~P9
IN													
OT													
D													

- When input control "EN" = 1, this instruction will readout one digit data from the 4 input points starting from IN (IN0~IN3). It takes 4 scans to read out a group of 4-digit BCD values (0000~9999) and store them into D register. With a 32-bit operand, each scan can get 2 digits of data by reading the additional digit from IN4~IN7 and store it in the D+1 register. Each bit of OT0~OT3 will sequentially set to 1 and get the digit data respectively into 10^0 (ones), 10^1 (tens), 10^2 (hundreds), and 10^3 (thousands). As long as EN is 1, PLC will scan and read out in continuous cycles. When each complete cycle is finished (i.e. the 4 digit readout of $10^0\sim10^3$ is completed), the readout completed flag "DN" is set to 1. However, it is only kept for one scan. If any digital readout value is not within the range of 0~9 (BCD), then reading error "ERR" will be set to 1 and the value of that group of digits will be set to 0000.
- The output points must be transistor outputs.



- In this example, when X10 is 1, then the numeric value of the thumb wheel switch (5678 in this example) will be read out and stored into the R0 register.
- The bits (8,4,2,1) with same digit should be connect together and series with a diode (as shown in diagram below).
- With 32-bit operand a set of similar thumb wheel switch may be added to X4~X7 (Y0~Y3 are shared with another group).



FUN 79 D 7SGDL	7-SEGMENT OUTPUT WITH LATCH	FUN 79 D 7SGDL
---	------------------------------------	---

Ladder symbol

Execution control — EN

79D.7SGDL

S :

OT :

N :

WR :

DN — Output complete

S : Register storing the data (BCD) to be displayed

OT : Starting number of scanning output

N : Specify signal output and polarity of latch

WR : Working register, it can't repeat in use

S may combine with V · Z · P0~P9 to serve indirect addressing application

Range	Y	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	Y0 Y240	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16-bit number	V · Z P0~P9
S			○	○	○	○	○	○	○	○	○	○	○	○	○
OT	○														
N														0~3	

- When input control "EN" = 1, the 4 nibbles of the S register, from digit 0 to digit 3, are sequentially sent out to the 4 output points, OT0~OT3. While output the digit data, the latch signal of that digit (OT4 corresponds to digit 0, OT5 corresponds to digit 1, etc...) at the same time is also sent out so that the digital value will be loaded and latched into the 7-segment display respectively.
- When in D (32-bit) instruction, nibbles 0~3 from the S register, and nibbles 0~3 from the S+1 register are transferred separately to OT0~OT3 and OT8~OT11. Because they are transferred at the same time, they can use the same latch signal. 16-bit instructions do not use OT8~OT11.
- As long as "EN" remains 1, PLC will execute the transfer cyclically. After each transfer of a complete group of numerical values (nibbles 0~3 or 0~7), the output completed flag "DN" will set to 1. However, it will only be kept for 1 scan.

X0

EN

79D.7SGDL

S : R0


OT : Y0

N : 2


WR : D0

DN — ()

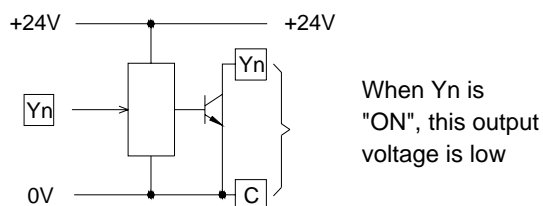
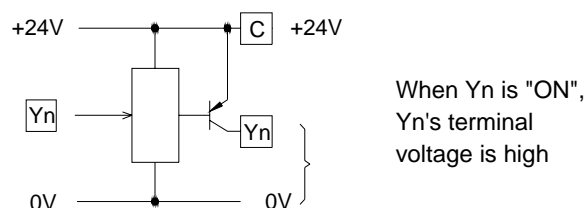
- In this example, when X0=1, the 4 nibbles of R0 will be transferred to the first group 7-segment display in the diagram below. The 4 nibbles of R1 will be transferred to the second group 7-segment display.

FUN 79 
7SGDL

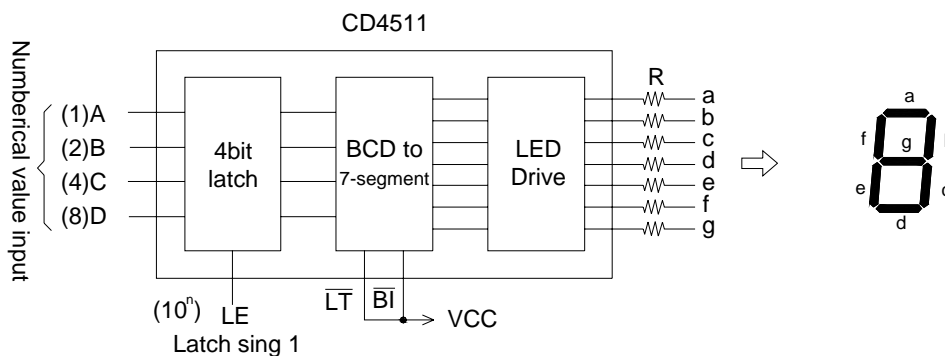
7-SEGMENT OUTPUT WITH LATCH

FUN 79 
7SGDL

- FATEK PLC's transistor output has both a negative logic transistor output (NPN transistor - when the output status is ON, the terminal voltage of the transistor output is low), and a positive logic transistor output (PNP - when the output status is ON, the terminal voltage of the transistor output is high). Their structure is as follows:

FBs-PLC negative logic output (NPN transistor)FBs-PLC positive logic output (PNP transistor)

- The data inputs (8,4,2,1) and latch signals of the 7-segment displays on the shelf for positive and negative logic are all available. For example, for numerical value "8", the positive logic input should be 1000, and the negative logic input 0111. Similarly, when the latch signal is 0, the positive logic latch permits the display numerical values to enter through the latch (i.e. be loaded). When the latch signal is 1, the numerical values in the latch are latched (maintained), and with negative logic they are not. The following diagram of a CD-4511 7-segment display IC is an example of a positive logic numerical value input with latch.



- Because the PLC output and the 7-segment display input polarity can be positive and negative logic. Therefore, the polarities between output and input must be coordinated to get the correct result. This instruction uses N to specify the polarity relation between the PLC transistor output, and the 7-segment display. The table below shows all the possibility.

Numerical value input (8~1)	Latch signal (10 ⁰ -10 ³)	Value of N
Same	Same	0
	Different	1
Different	Same	2
	Different	3

- In the diagram above, CD4511 is used as an example. If use NPN output, the data input polarity is different to PLC, and its latch input polarity is the same as PLC, so N value should chosen as 2.

FUN 80
MUXI

MULTIPLEX INPUT

FUN 80
MUXI

Ladder symbol

Execution control — EN

80.MUXI

IN :

OT :

N :

D :

WR :

DN — Execution completed

IN : Multiplex input point number

OT : Multiplex output point number
(must be transistor output point)

N : Multiplex input lines (2~8)

D : Register for storing results

D may combine with V, Z, P0~P9 to serve indirect address application

Range	X	Y	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	K	XR
Ope- rand	X0 X240	Y0 Y240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	2 8	V · Z P0~P0
	IN	○												
OT		○												
N													○	
D			○	○	○	○	○	○	○	○*	○*	○		○

- This instruction uses the multiplex method to read out N lines of input status from 8 consecutive input points (IN0~IN7) starting from the input point specified by IN. With this method we can obtain 8xN input status, but only need to use 8 input points and N output points.
- The multiplex scanning method goes through N output points starting from the OT output point. Each scan one of the N bits will set to 1 and the corresponding line will be selected. OT0 responsible for first line, while OT1 responsible for second line, etc. Until it read all the N lines the 8xN status that has been read out is then stored into the register starting at D, and the execution completed flag "DN" is set as 1 (but is only kept for one scanning period).
- With every scan, this instruction retrieves a line for 8 input status, so N lines require N scan cycles before they can be completed.

X0

—|

EN

80.MUXI

IN : X24

OT : Y16

N : 4

D : WM0

WR : D0

DN

—

()

Fourth line

Third line

Second line

First line

M24

M25

M26

M27

M28

M29

M30

M31

M16

M17

M18

M19

M20

M21

M22

M23

M8

M9

M10

M11

M12

M13

M14

M15

M0

M1

M2

M3

M4

M5

M6

M7

S/S

X24

X25

X26

X27

X28

X29

X30

X31

PLC NPN transistor output

24V

C

Y16

Y17

Y18

Y19

Y20









Y21

Y22

Y23

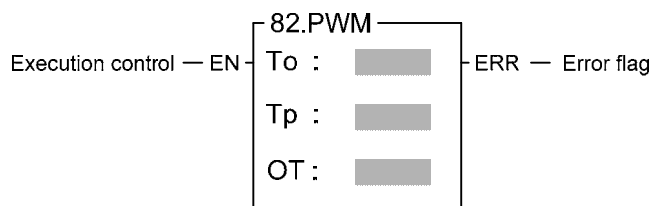
- This example retrieves 4 linesx8 points of input, 32 point status in all. They are stored into the 32-bit register of DWM0 (M0~M31).

7-75

FUN 81 		PULSE OUTPUT												FUN 81 																																																																																																																	
<div><div><div><div>Ladder symbol</div><div><div>81D.PLSO</div><div><div>Output control — EN</div><div>Pause control — PAU</div><div>Up/Down direction — U/D Or DIR</div></div><div><div>MD : </div><div>Fr : </div><div>PC : </div><div>UY:or CK </div><div>DY:or DR </div><div>HO : </div></div><div><div>OUT — Output go</div><div>DN — Output completed</div><div>ERR — Error</div></div></div><div><div>MD : Output mode selection</div><div>Fr : Pulse frequency</div><div>PC : Output pulse count</div><div>UY : Up pulse output point (MD=0).</div><div>DY : Down pulse output point (MD=0).</div><div>HO : Cumulative output pulse register. (Can be not assigned).</div><div>CK : Pulse output point (MD=1).</div><div>DR : Up/Down output point (MD=1).</div><div>DIR: 1- up; 0- down.</div></div></div></div><table><tr><th>Range</th><th>Y</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th></tr><tr><th>Ope- rand</th><th>Yn of Main Unit</th><th>WX0 WX240</th><th>WY0 WY240</th><th>WM0 WM1896</th><th>WS0 WS984</th><th>T0 T255</th><th>C0 C255</th><th>R0 R3839</th><th>R3904 R3967</th><th>R3968 R4167</th><th>R5000 R8071</th><th>D0 D4095</th><th>16/32-bit +/- number</th></tr><tr><td>MD</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>0~1</td></tr><tr><td>Fr</td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>8~2000</td></tr><tr><td>PC</td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td></tr><tr><td>UY · CK</td><td>○</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>DY · DR</td><td>○</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>HO</td><td></td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○*</td><td>○*</td><td>○</td><td></td></tr></table><div><ul style="list-style-type: none">When MD=0, this instruction performs the pulse output control as following:Whenever the output control “EN” changes from 0→1, it first performs the reset action, which is to clear the output flag “OUT” and “DN” as well as the pulse out register HO to be 0. It gets the pulse frequency and output pulse count values, and reads status of up and down direction “U/D”, so as to determine the direction to be upward or downward. As the reset finished, this instruction will check the input status of pause output “PAU”. No action will be taken if the pause output is 1 (output pause). If the PAU is 0, it will start to output the ON/OFF pulse with 50% duty at the frequency Fr to the UY(U/D=1) or DY(U/D=0) point. It will increment the value of HO register each time when a pulse is output, and will stop the output when HO register's pulse count is equal to or greater than the cumulative pulse count of PC register and set the output complete flag “DN” to 1. During the time when output pulse is transmitting the output transmitting flag “OUT” will be set to 1, otherwise it will be 0.Once it starts to transmit pulse, the output control “EN” should kept to 1. If it is changed to 0, it will stop the pulse sending (output point become OFF) and the flag “OUT” changes back to 0, but the other status or data will keep unchanged. However, when its “EN” changes again from 0 to 1, it will lead to a reset action and treat as a new start; the entire procedure will be restarted again.If you want to pause the pulse output and not to restart the entire procedure, the ‘pause output’ “PAU” input can be used to pause it. When “PAU” =1, this instruction will pause the pulse transmitting (output point is OFF, flag “OUT” change back to 0 and the other status or data keeps unchanged). As it waits until the “PAU” changes back from 1 to 0, this instruction will return to the status before it is paused and continues the pulse transmitting output.During the pulse transmission, this instruction will keep monitoring the value of pulse frequency Fr and output pulse count PC. Therefore, as long as the pulse output is not finished, it may allow the changing of the pulse frequency and pulse count. However, the up/down direction “U/D” status will be got only once when it takes the reset action (“EN” changes from 0→1), and will keep the status until the pulse output completed or another reset occur. That is to say, except that at the very moment of reset, the change of “U/D” does not influence the operation of this instruction.The main purpose of this instruction is to drive the stepping motor with the UY (upward) and DY (downward) two directional pulses control, so as to help you control the forward or reverse rotating of stepping motor. Nevertheless, if you need only single direction revolving, you can assign just one of the UY or DY (which will save one output point), and leaving the other output blank. In such case, the instruction will ignore the up/down input status of “U/D”, and the output pulse will send to the output point you assigned.</div></div>																Range	Y	WX	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	K	Ope- rand	Yn of Main Unit	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number	MD													0~1	Fr		○	○	○	○	○	○	○	○	○	○	○	8~2000	PC		○	○	○	○	○	○	○	○	○	○	○	○	UY · CK	○													DY · DR	○													HO			○	○	○	○	○	○	○	○*	○*	○	
Range	Y	WX	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	K																																																																																																																		
Ope- rand	Yn of Main Unit	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number																																																																																																																		
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Fr		○	○	○	○	○	○	○	○	○	○	○	8~2000																																																																																																																		
PC		○	○	○	○	○	○	○	○	○	○	○	○																																																																																																																		
UY · CK	○																																																																																																																														
DY · DR	○																																																																																																																														
HO			○	○	○	○	○	○	○	○*	○*	○																																																																																																																			

FUN 81 D PLSO	PULSE OUTPUT	FUN 81 D PLSO
<ul style="list-style-type: none">When MD=1, the pulse output will reflect on the control output DIR (pulse direction. DIR=1, up; DIR=0, down) and CK (pulse output).This instruction can only be used once, and UY (CK) and DY (DR) must be transistor output point on the PLC main unit.The effective range of output pulse count PC for 16 bit operand is 0~32767. For the 32 bit operand(instruction), it is 0~2147483647. If the PC value = 0, it is treated as infinite pulse count, and this instruction will transmit pulses without end with HO value and "DN" flag set at 0 all the time. The effective range of pulse frequency (Fr) is 8~2000. If the value PC or Fr exceeds the range, this instruction will not be carried out and the error flag "ERR" will set to 1.		
<div><div><div><div>X0</div><div>X1</div><div>X2</div></div><div>EN</div><div>PAU</div><div>U/D</div></div><div><div>81D.PLSO</div><div>MD : 0</div><div>Fr : R 0</div><div>PC : R 1</div><div>UY : Y 0</div><div>DY : Y 1</div><div>HO : R 5</div></div><div><div>OUT—()</div><div>DN —()</div><div>ERR—</div></div></div> <div><div>M0</div><div>M1</div></div> <div><ul style="list-style-type: none">In this example, the program controls the stepping motor to drive forward for 80 pulses (steps) at the speed of 100Hz first, and then makes it turn reverse for 40 pulses the speed of 50Hz. Make sure that the up/down direction, frequency Fr and the pulse count PC must be set before the reset take action("EN" changes from 0→1).</div>		
<div><div><div>Turn forward 100Hz going 80 steps</div><div>Turn reverse 50Hz going 40 steps</div></div><div><div>Reset enable</div><div>re-start</div><div>Stop (finished)</div><div>Reset</div><div>Start</div><div>Stop (finished)</div></div><div><div>Output enable X0</div><div>Pause X1</div><div>Direction X2</div><div>Up-pulse Y0</div><div>Down-pulse Y1</div><div>Under output M0</div><div>Output done M1</div><div>Frequency R0</div><div>Pulse to output R1</div><div>Output pulse count R5</div></div><div><div>Forward</div><div>Reverse</div><div>1</div><div>2</div><div>76</div><div>77</div><div>78</div><div>79</div><div>80</div><div>1</div><div>2</div><div>40</div><div>0</div><div>1</div><div>2</div><div>39</div><div>40</div></div><div><div>100</div><div>50</div><div>80</div><div>40</div></div><div><div>0</div><div>1</div><div>2</div><div>75</div><div>76</div><div>77</div><div>78</div><div>79</div><div>80</div><div>0</div><div>1</div><div>2</div><div>39</div><div>40</div></div></div>		

FUN 82 PWM	PULSE WIDTH MODULATION	FUN 82 PWM
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Ladder symbol

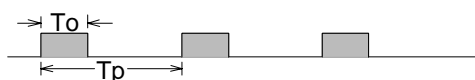
To : Pulse ON width
(0~32767mS)

Tp : Pulse period
(1~32676mS)

OT: Pulse output point

Range	Y	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K
Operand	Yn of main unit	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	0 32767
To		○	○	○	○	○	○	○	○	○	○	○	○	○
Tp		○	○	○	○	○	○	○	○	○	○	○	○	○
OT	○													












- When execution control "EN" = 1, will send the pulse to output point OT with the "ON" state for To ms and period as Tp. OT must be a transistor output point on the main unit. When "EN" is 0, the output point will be OFF.



- The units for Tp and To are mS, resolution is 1 mS. The minimum value for To is 0 (under such case the output point OT will always be OFF), and its maximum value is the same as Tp (under such case the output point OT will always be on). If To > Tp there will be an error, this instruction will not be carried out, and the error flag "ERR" will set to 1.
- This instruction can only be used once.

FUN 83 SPD	SPEED DETECTION														FUN 83 SPD																																																																																									
<div><div><div><div>Ladder symbol</div><div><div>Detection control — EN</div><div><div>83.SPD</div><div><div>S : <div></div></div><div>TI : <div></div></div><div>D : <div></div></div></div><div>OVF — Overflow</div></div></div><div><div>S : Pulse input point for speed detection</div><div>TI : Sampling duration (units in mS)</div><div>D : Register storing results</div></div></div><table><tr><th>Range</th><th>X</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th></tr><tr><td rowspan="2">Ope- rand</td><td>X0</td><td>WX0</td><td>WY0</td><td>WM0</td><td>WS0</td><td>T0</td><td>C0</td><td>R0</td><td>R3840</td><td>R3904</td><td>R3968</td><td>R5000</td><td>D0</td><td>1</td></tr><tr><td>X7</td><td>WX240</td><td>WY240</td><td>WM1896</td><td>WS984</td><td>T255</td><td>C255</td><td>R3839</td><td>R3903</td><td>R3967</td><td>R4167</td><td>R8071</td><td>D4095</td><td>32767</td></tr><tr><td>S</td><td>○</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>TI</td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td></tr><tr><td>D</td><td></td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○*</td><td>○*</td><td>○</td><td></td></tr></table><div><ul style="list-style-type: none">• This instruction uses the interrupt feature of the 8 high speed input points (X0~X7) on the PLC main unit to detect the frequency of the input signal. Within a specific sampling time (TI), it will calculate the input pulse count for S input point, and indirectly find the revolution speed of rotating devices (such as motors).• While use this instruction to detect the rotating speed of devices, The application should design to generate more pulse per revolution in order to get better result, but the sum of input frequency of all detected signals should under 5KHz, otherwise the WDT may occur.• The D register for storing results uses 3 successive 16-bit registers starting from D (D0~D2). Besides D0 which is used to store counting results, D1 and D2 are used to store current counting values and sampling duration.• When detection control "EN" = 1, it starts to calculate the pulse count for the S input point, which can be shown in D1 register. Meanwhile the sampling timer (D2) is switched on and keeps counting until the value of D2 is reach to the sampling period (TI). The final counted value is stored into the D0 register, and then a new counting cycle is started again. The sampling counting will go on repeating until "EN" = 0.• Because D0 only has 16 bits, so the maximum count is 32767. If the sampling period is too long or the input pulse is too fast then the counted value may exceed 32767, under that case the overflow flag will set to 1, and the counting action will stop.• Because the sampling period TI is already known and if every revolution of attached rotating device produces "n" pulses, then the following equation can be used to get the revolution<div><div>speed : $N = \frac{(D0) \times 60}{n \times TI} \times 10^3 \quad (\text{rpm})$</div><div><div><div>X20</div><div>EN</div><div><div>83.SPD</div><div><div>S : X 0</div><div>TI : 1000</div><div>D : R 0</div></div><div>OVF</div></div></div></div><ul style="list-style-type: none">• In the above example, if every revolution of the rotating device produces 20 pulses (n = 20), and the R0 value is 200, then the revolution per minute speed "N" is as<div><div>follows : $N = \frac{(200) \times 60}{60 \times 1000} \times 10^3 = 200 \text{ rpm}$</div></div></div><div><div><div><div>X20</div><div>X0</div><div>1000</div><div>R2</div><div>0</div><div>1000mS</div><div>1000mS</div><div>1000mS</div><div>R1</div><div>0</div><div>a</div><div>b</div><div>c</div><div>R0</div><div>R1a</div><div>R1b</div><div>R1c</div></div></div></div></div></div></div>																Range	X	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	Ope- rand	X0	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	1	X7	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	32767	S	○														TI		○	○	○	○	○	○	○	○	○	○	○	○	○	D			○	○	○	○	○	○	○	○	○*	○*	○	
Range	X	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K																																																																																										
Ope- rand	X0	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	1																																																																																										
	X7	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	32767																																																																																										
S	○																																																																																																							
TI		○	○	○	○	○	○	○	○	○	○	○	○	○																																																																																										
D			○	○	○	○	○	○	○	○	○*	○*	○																																																																																											

FUN 84 TDSP	PATTERN CONVERSION FOR 16/7-SEGMENT DISPLAY	FUN 84 TDSP																																																								
<div><div><div><div>Ladder symbol</div><div><div>84.TDSP</div><div><div>Execution control — EN</div><div>Md : <div></div></div><div>S : <div></div></div><div>All OFF Input control — OFF</div><div>Ns : <div></div></div><div>NI : <div></div></div><div>All ON Input control — ON</div><div>D : <div></div></div><div>Nd : <div></div></div></div></div><div><div>Md : Operation Mode, 0~3</div><div>S : Starting address of being converted characters</div><div>Ns : Start of source character, 0~63</div><div>NI : Length of character, 1~64</div><div>D : Starting address to store the converted pattern</div><div>Nd : Start pointer while storing</div><div>S operand can be combined with V、Z、P0~P9 index registers for indirect addressing</div></div></div><div><table><tr><th>Range</th><th>HR</th><th>OR</th><th>ROR</th><th>DR</th><th>K</th><th>Index</th></tr><tr><td>Oper- and</td><td>R0 R3839</td><td>R3904 R3967</td><td>R5000 R8071</td><td>D0 D3999</td><td>Positive integer 16/32-bit</td><td>V、Z、 P0~P9</td></tr><tr><td>Md</td><td></td><td></td><td></td><td></td><td>0 ~ 3</td><td></td></tr><tr><td>S</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td></tr><tr><td>Ns</td><td>○</td><td>○</td><td>○</td><td>○</td><td>0 ~ 63</td><td></td></tr><tr><td>NI</td><td>○</td><td>○</td><td>○</td><td>○</td><td>1 ~ 64</td><td></td></tr><tr><td>D</td><td>○</td><td>○</td><td>○*</td><td>○</td><td></td><td></td></tr><tr><td>Nd</td><td>○</td><td>○</td><td>○*</td><td>○</td><td>0 ~ 63</td><td></td></tr></table></div></div><div><div><div>● This instruction is used for FBs-7SG1/FBs-7SG2 module’s application. It can convert the source alphanumeric characters into display patterns suited for 16 segment encoded mode display or perform the leading zero substitution of the packed BCD number for non-decoded mode 7 segment display.</div><div>● When execution control “EN” =1, and input “OFF” = 0, input “ON”=0, if Md=0, this instruction will perform the display pattern conversion, where S is the starting address storing the being converted characters, Ns is the pointer to locate the starting address character, NI tells the length of being converted characters, and D is the starting address to store the converted result.</div><div>Byte 0 of S is the “1st” displaying character, byte 1 of S is the 2nd displaying character,.....</div><div>Ns is the pointer to tell where the start character is.</div><div>After execution, each 8-bit character of the source will be converted into the corresponding 16-bit display pattern.</div><div>● When input “OFF” = 1, all bits of display pattern will be ‘off’ if Md = 0, if Md=1, all BCD codes will be substituted by blank code (0F)</div><div>● When input “ON” = 1, all bits of display pattern will be ‘on’ if Md=0. If Md=1, all BCD codes will be substituted by code 8(all light).</div><div>● Please refer Chapter 16 “FBs-7SG display module” for more detail description.</div></div></div></div>			Range	HR	OR	ROR	DR	K	Index	Oper- and	R0 R3839	R3904 R3967	R5000 R8071	D0 D3999	Positive integer 16/32-bit	V、Z、 P0~P9	Md					0 ~ 3		S	○	○	○	○		○	Ns	○	○	○	○	0 ~ 63		NI	○	○	○	○	1 ~ 64		D	○	○	○*	○			Nd	○	○	○*	○	0 ~ 63	
Range	HR	OR	ROR	DR	K	Index																																																				
Oper- and	R0 R3839	R3904 R3967	R5000 R8071	D0 D3999	Positive integer 16/32-bit	V、Z、 P0~P9																																																				
Md					0 ~ 3																																																					
S	○	○	○	○		○																																																				
Ns	○	○	○	○	0 ~ 63																																																					
NI	○	○	○	○	1 ~ 64																																																					
D	○	○	○*	○																																																						
Nd	○	○	○*	○	0 ~ 63																																																					

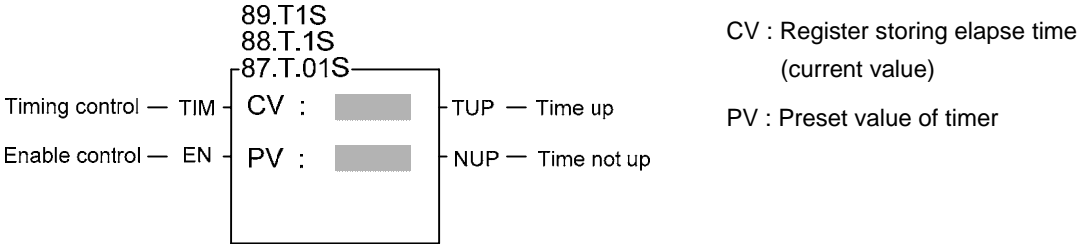
FUN 86 TPCTL		PID TEMPERATURE CONTROL INSTRUCTION				FUN 86 TPCTL																																																																															
		<p><u>Ladder symbol</u></p> <p>86.TPCTL</p> <div><div>Execution control — EN</div><div>Heating/Cooling — H/C</div></div> <div><div>Md : </div><div>Yn : </div><div>Sn : </div><div>Zn : </div><div>Sv : </div><div>Os : </div><div>PR : </div><div>IR : </div><div>DR : </div><div>OR : </div><div>WR : </div></div> <div><div>ERR — Parameter error</div><div>ALM — Temperature Control warning</div></div>																																																																																			
		<p>Md: Selection of PID method =0, Modified minimum overshoot method =1, Universal PID method</p> <p>Yn: Starting address of PID ON/OFF output; it takes Zn points.</p> <p>Sn: Starting point of PID control of this instruction; Sn = 0~31.</p> <p>Zn: Number of the PID control of this instruction; 1≤Sn+Zn≤32</p> <p>Sv: Starting register of the set point: it takes Zn registers.</p> <p>Os: Starting register of the in-zone offset; it takes Zn registers.</p> <p>PR: Starting register of the gain (Kc): it takes Zn registers.</p> <p>IR: Starting register of integral tuning constant (Ti);it takes Zn registers..</p> <p>DR: Starting register of derivative tuning constant (Td); it takes Zn registers.</p> <p>OR: Starting register of the PID analog output. it takes Zn registers.</p> <p>WR: Starting of working register for this instruction. It takes 9 registers and can't be repeated in using.</p>																																																																																			
		<table><tr><th>Range</th><th>Y</th><th>HR</th><th>ROR</th><th>DR</th><th>K</th></tr><tr><td>Oper- and</td><td>Y0 Y255</td><td>R0 R3839</td><td>R5000 R8071</td><td>D0 D3999</td><td></td></tr><tr><td>Md</td><td></td><td></td><td></td><td></td><td>0~1</td></tr><tr><td>Yn</td><td>○</td><td></td><td></td><td></td><td></td></tr><tr><td>Sn</td><td></td><td></td><td></td><td></td><td>0~31</td></tr><tr><td>Zn</td><td></td><td></td><td></td><td></td><td>1~32</td></tr><tr><td>Sv</td><td></td><td>○</td><td>○*</td><td>○</td><td></td></tr><tr><td>Os</td><td></td><td>○</td><td>○*</td><td>○</td><td></td></tr><tr><td>PR</td><td></td><td>○</td><td>○*</td><td>○</td><td></td></tr><tr><td>IR</td><td></td><td>○</td><td>○*</td><td>○</td><td></td></tr><tr><td>DR</td><td></td><td>○</td><td>○*</td><td>○</td><td></td></tr><tr><td>OR</td><td></td><td>○</td><td>○*</td><td>○</td><td></td></tr><tr><td>WR</td><td></td><td>○</td><td>○*</td><td>○</td><td></td></tr></table>				Range	Y	HR	ROR	DR	K	Oper- and	Y0 Y255	R0 R3839	R5000 R8071	D0 D3999		Md					0~1	Yn	○					Sn					0~31	Zn					1~32	Sv		○	○*	○		Os		○	○*	○		PR		○	○*	○		IR		○	○*	○		DR		○	○*	○		OR		○	○*	○		WR		○	○*	○			
Range	Y	HR	ROR	DR	K																																																																																
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PR		○	○*	○																																																																																	
IR		○	○*	○																																																																																	
DR		○	○*	○																																																																																	
OR		○	○*	○																																																																																	
WR		○	○*	○																																																																																	
<ul style="list-style-type: none">● By employing the temperature module and table editing method to get the current value of temperature and let it be as so called Process Variable (PV); after the calculation of software PID expression, it will respond the error with an output signal according to the setting of Set Point (SP), the error's integral and the rate of change of the process variable. Through the closed loop operation, the steady state of the process may be expected.● Convert the output of PID calculation to be the time proportional ON/OFF (PWM) output, and via transistor output to control the SSR for heating or cooling process; this is a good performance and very low cost solution.● Through the analog output module (D/A module), the output of PID calculation may control the SCR or proportional value to get more precise process control.● Please refer to Chapter 20 “Temperature Measurement of FBs-PLC and PID Control” for more details.																																																																																					

FUN 86 TPCTL	PID TEMPERATURE CONTROL INSTRUCTION	FUN 86 TPCTL
	<p>● PID temperature control (FUN86) instruction supports user defined starting address of temperature reading value for more flexibility in temperature control application</p> <ul style="list-style-type: none"> · R4003=A55AH, starting address of temperature reading value is defined by R4004 =other values, starting address of temperature reading value is defined by temperature configuration screen · R4004=10000~13839, it defines R0~R3839 is the starting address of temperature reading value as the process variables for PID control =20000~23999, it defines D0~D3999 is the starting address of temperature reading value as the process variables for PID control =other values, starting address of temperature reading value is defined by temperature configuration screen 	

Cumulative Timer Instructions

FUN87 T.01S FUN88 T.1S FUN89 T1S	ACCUMULATIVE TIMER	FUN87 T.01S FUN88 T.1S FUN89 T1S
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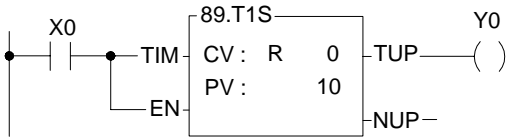
Ladder symbol



Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	0
	WX240	WY240	WM1896	WS984	T255	C199	R3839	R3903	R3967	R4167	R8071	D4095	32767
CV		○	○	○	○	○	○	○	○	○*	○*	○	
PV	○	○	○	○	○	○	○	○	○	○	○	○	○

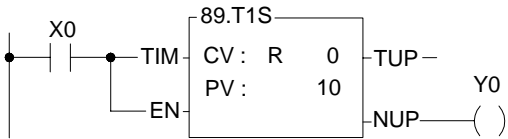
- The operation for this instruction is the same as that for the basic timer (T0~T255), except that the basic timer only has a "timing control" input - when its input is 1 it starts timing, and when input is 0 it get clear. Every time the input changes, it starts timing again and is unable to accumulate. Timing with this instruction is only permissible when enable control "EN" = 1. With this instruction, when timing control "TIM" is 1, it is the same as a basic timer, but when "TIM" is 0, it does not clear, but keeps the current value. If the timer need to clear, then change enable control "EN" to 0. When timing control "TIM" is once again to be 1, it will continue to accumulate from the previous value when the timer last paused. In addition, this instruction also has two outputs, "Time up TUP" (when time up it is 1, usually it is 0) and "Time not up" (usually it is 1, when time is up it is 0). Users can utilize input and output combinations to produce timers with various different functions. For example:

- On delay energizing timer:

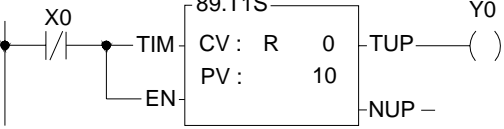
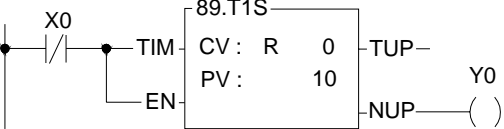
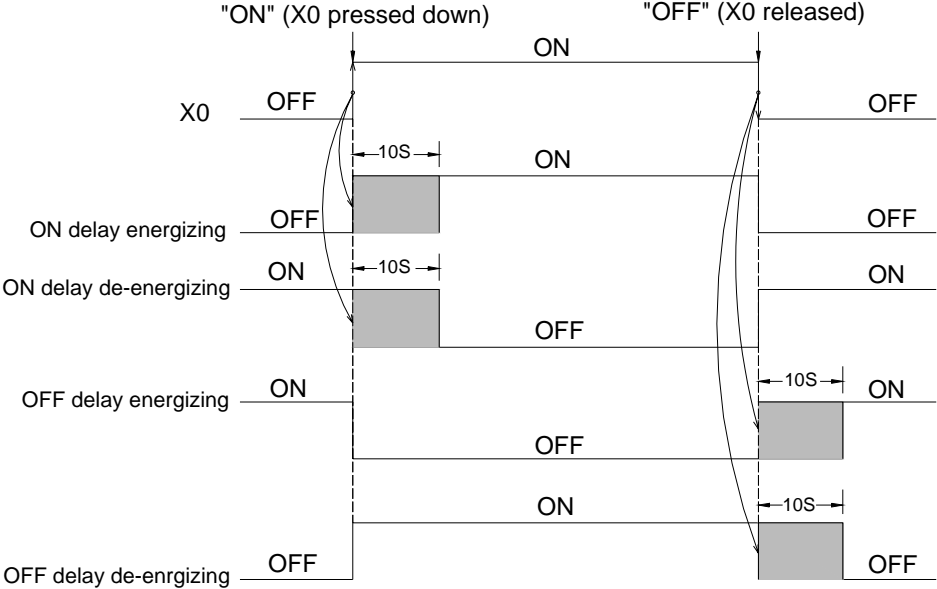


- This timer's output (Y0 in this example) is normally not energized. When this timer's input control (X0 in this example) is activated (ON), only after delay by 10 sec will output Y0 become energized (ON).





- On delay de-energizing timer:






- The output Y0 of this timer is usually energized. When this timer's input control X0 is on, only after delay by 10 sec will the output become de-energized (OFF).

FUN87 T.01S FUN88 T.1S FUN89 T1S	ACCUMULATIVE TIMER	FUN87 T.01S FUN88 T.1S FUN89 T1S
<div><ul style="list-style-type: none">Off delay energizing timer:<div></div><ul style="list-style-type: none">This timer's output Y0 is usually de-energized. When this timer's input control X0 is off, only after delay by 10 sec will output Y0 become energized (ON).Off delay de-energizing timer:<div></div><ul style="list-style-type: none">This timer's output Y0 is usually energized. When this timer's timing control X0 is off, only after delay by 10 sec will output Y0 become de-energized (OFF).<div><ul style="list-style-type: none">The diagram below shows the relation on input and output for the above 4 kinds of timers.<div></div></div></div>		

Watchdog Timer Instructions

FUN 90  WDT	WATCHDOG TIMER	FUN 90  WDT
<div><div><div><div><div></div><div>Ladder symbol</div></div><div>Execution control—EN — <div><div>90P.</div><div>WDT</div><div>N</div></div></div></div><div>N : The watchdog time. The range of N is 5~120, unit in 10mS (i.e. 50ms~1.2 sec)</div></div></div>		
<ul style="list-style-type: none">● When execution control "EN" = 1 or transition from 0 to 1( instruction), will set the watchdog time to Nx10ms. If the scan time exceeds this preset time, PLC will shut down and not execute the application program.● The WDT feature is designed mainly as a safety consideration from the system view for the application. For example, if the CPU of PLC is suddenly damaged, and there is no way to execute the program or refresh I/O, then after the WDT time expired, the WDT will automatically switch off all the I/Os, so as to ensure safety. In certain applications, if the scan time is too long, it may cause safety problems or problems of non-conformance with control requirements. This instruction can used to establish the limitation of the scan time that you require.● Once the WDT time has been set it will always be kept, and there is no need to set it again on each scan. Therefore, in practice this instruction should use the  instruction.● Default WDT time is 0.25 sec.● For the operation principles of WDT please refer to the RSWDT(FUN 91) instruction.		

FUN 91  RSWDT	RESET WATCHDOG TIMER	FUN 91  RSWDT
	<p style="text-align: center;"><u>Ladder symbol</u></p> <div style="display: flex; align-items: center; justify-content: space-around;"> <div style="text-align: center;"> <p>Execution control—EN</p> <div style="border: 1px solid black; padding: 5px; display: inline-block;"> <p>91P.</p> <div style="background-color: #cccccc; padding: 2px 10px; margin-top: 5px;">RSWDT</div> </div> </div> <div style="text-align: center;"> <p>This instruction has no operand.</p> </div> </div>	
<ul style="list-style-type: none"> When execution control "EN" = 1 or from 0 to 1 ( instruction), the WDT timer will be reset (i.e. WDT will start timing again from 0). The functions of WDT have already been described in FUN90 (WDT instruction). The operation principles of watch dog timer are as follows: The watchdog timer is normally implemented by a hardware one-shot timer (it can not be software, otherwise if CPU fail, the timer becomes ineffective, and safeguards are quite impossible). "One-shot" means that after triggered the timer once, the timing value will immediately be reset to 0 and timing will restart. If WDT has begun timing, and never triggered it again, then the WDT timing value will continue accumulating until it reach the preset value of N, at that time WDT will be activated, and PLC will be shut down. If trigger the WDT once every time before the WDT time N has been reached, then WDT will never be activated. PLC can use this feature to ensure the safety of the system. Each time when PLC enters into system housekeeping after finished the program scanning and I/O refresh, it will usually trigger WDT once, so if the system functions normally and scan time does not exceed WDT time then WDT is never activated. However, if CPU is damaged and unable to trigger WDT, or the scan time is too long, then there will not be enough time to trigger WDT within the period N, WDT will be activated and will shut off PLC. In some applications, when you set the WDT time (FUN90) to desire, the scan time of your program in certain situations may temporarily exceed the preset time of WDT. This situation can be anticipated and allowed for, and you naturally do not wish PLC to shut down for this reason. You can use this instruction to trigger WDT once and avoid the activation of WDT. This is the main purpose of this instruction. 		

FUN 92 D P HSCTR	HARDWARE HIGH SPEED COUNTER CURRENT VALUE (CV) ACCESS	FUN 92 D P HSCTR
<div><div><div>Ladder symbol</div><div><div>Readout control — EN</div><div><div>92P.</div><div><div>HSCTR</div><div>CN</div></div></div></div></div><div><div>CN : Hardware high speed counter number</div><div>0: HSC0 or HST0</div><div>1: HSC1 or HST1</div><div>2: HSC2 or HST2</div><div>3: HSC3 or HST3</div><div>4: HSTA</div></div></div>		
<div><div><ul style="list-style-type: none">The HSC0~HSC3 counters of FBs-PLC are 4 sets of 32bit high speed counter with the variety counting modes such as up/down pulse, pulse-direction, AB-phase. All the 4 high speed counters are built in the ASIC hardware and could perform count, compare, and send interrupt independently without the intervention of the CPU. In contrast to the software high speed counters HSC4~HSC7, which employ interrupt method to request for CPU processing, hence if there are many counting signals or the counting frequency is high, the PLC performance (scanning speed) will be degraded dramatically. Since the current values CV of HSC0~HSC3 are built in the internal hardware circuits of ASIC, the user control program (ladder diagram) cannot retrieve them directly from ASIC. Therefore, it must employ this instruction to get the CV value from hardware HSC and put it into the register which control program can access. The following is the arrangement of CV, PV in ASIC and their corresponding CV, PV registers of PLC for HSC0~HSC3.</div><div><div><div><div>PLC register</div><div><div>HSC0</div><div><div>CV register</div><div>DR4096</div><div>H</div><div>L</div></div><div><div>PV register</div><div>DR4098</div><div>H</div><div>L</div></div></div><div><div>HSC1</div><div><div>CV register</div><div>DR4100</div><div>H</div><div>L</div></div><div><div>PV register</div><div>DR4102</div><div>H</div><div>L</div></div></div><div><div>HSC2</div><div><div>CV register</div><div>DR4104</div><div>H</div><div>L</div></div><div><div>PV register</div><div>DR4106</div><div>H</div><div>L</div></div></div><div><div>HSC3</div><div><div>CV register</div><div>DR4108</div><div>H</div><div>L</div></div><div><div>PV register</div><div>DR4110</div><div>H</div><div>L</div></div></div><div><div>HSTA</div><div><div>CV register</div><div>DR4152</div><div>H</div><div>L</div></div><div><div>PV register</div><div>R4154</div><div></div><div></div></div></div></div><div><div>ASIC</div><div><div>CV</div><div></div></div><div><div>PV</div><div></div></div><div><div>CV</div><div></div></div><div><div>PV</div><div></div></div><div><div>CV</div><div></div></div><div><div>PV</div><div></div></div><div><div>CV</div><div></div></div><div><div>PV</div><div></div></div><div><div>CV</div><div></div></div><div><div>PV</div><div></div></div></div></div><div><div><div><div>HSC0</div><div></div><div></div></div><div><div>HSC1</div><div></div><div></div></div><div><div>HSC2</div><div></div><div></div></div><div><div>HSC3</div><div></div><div></div></div><div><div>HSTA</div><div></div><div></div></div></div></div></div></div> <div><div><ul style="list-style-type: none">When access control “EN” =1 or changes from 0→1(P instruction), will gets the CV value of HSC designated by CN from ASIC and puts into the HSC corresponding CV register (i.e. the CV of HSC0 will be read and put into DR4096 or the CV of HSC1 will be read and put into DR4100).Although the PV within ASIC has a corresponding PV register in CPU, but it is not necessary to access it (actually it can't be) for that the PV value within ASIC comes from the PV register in CPU.HSTA is a timer, which use 0.1ms as its time base. The content of CV represents elapse time counting at 0.1mS tick.For detailed applications, please refer to Chapter 10 “The high speed counter and high speed timer of FBs-PLC”.</div></div>		

FUN 93 D P HSCTW	HARDWARE HIGH SPEED COUNTER CURRENT VALUE AND PRESET VALUE WRITING	FUN 93 D P HSCTW
<div><div><div>Ladder symbol</div><div><div>93DP.HSCTW</div><div>Write control—EN</div><div>S : <div></div></div><div>CN : <div></div></div><div>D : <div></div></div></div></div><div><div>S : The source data for writing</div><div>CN : Hardware high speed counter to be written</div><div>0: HSC0 or HST1</div><div>1: HSC1 or HST2</div><div>2: HSC2 or HST3</div><div>3: HSC3 or HST4</div><div>4: HSTA</div><div>D : Write target (0 represents CV, 1 represents PV)</div></div></div>		
<div><div><div><div><div>M0</div><div>↑</div><div>EN</div></div><div><div>93D.HSCTW</div><div>S : 0</div><div>CN : HSC0</div><div>D : CV</div></div></div><div><div><div>M0</div><div>↓</div><div>EN</div></div><div><div>92</div><div>HSCTR</div><div>HSC0</div></div></div><div><div><div>M1</div><div>↑</div><div>EN</div></div><div><div>93D.HSCTW</div><div>S : R500</div><div>CN : HSC0</div><div>D : PV</div></div></div></div><div><div><div>As the program in the left diagram, when M0 changes from 0→1, it clears the current value of HSC0 to 0, and writes into ASIC hardware through FUN93.</div><div>When M0 is 0, it reads out the current counting value.</div><div>When M1 changes from 0→1, it moves DR500 to DR4098, and writes the preset value into ASIC hardware through FUN93.</div><div>Whenever the current value equals to the DR500, The HSC0I interrupt sub program will be executed.</div></div></div></div>		



FUN 94 P ASCWR		ASCII WRITE												FUN 94 P ASCWR																																																																																				
<div><div><div><div>Ladder symbol</div><div><div>94P.ASCWR</div><div>Output control — EN — MD : <div></div> — ACT — Acting</div><div>Pause control — PAU — S : <div></div> — ERR — Error</div><div>Abort output — ABT — Pt : <div></div> — DN — Output completed</div></div></div><div><div>MD: Output mode =0, output to communication port1. others, reserved for future usage.</div><div>S : Starting register of file data.</div><div>Pt : Starting working register for this instruction instance. It taken up 8 registers and can't be reused in other part of program.</div></div></div></div>																																																																																																		
<table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th></tr><tr><td rowspan="2">Ope- rand</td><td>WX0</td><td>WY0</td><td>WM0</td><td>WS0</td><td>T0</td><td>C0</td><td>R0</td><td>R3840</td><td>R3904</td><td>R3967</td><td>R5000</td><td>D0</td><td>0</td></tr><tr><td>WX240</td><td>WY240</td><td>WM1896</td><td>WS984</td><td>T255</td><td>C255</td><td>R3839</td><td>R3903</td><td>R3967</td><td>R4167</td><td>R8071</td><td>D4095</td><td>1</td></tr><tr><td>MD</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>○</td></tr><tr><td>S</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td></tr><tr><td>Pt</td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td><td>○*</td><td>○*</td><td>○</td><td></td></tr></table>																Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3967	R5000	D0	0	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	1	MD													○	S	○	○	○	○	○	○	○	○	○	○	○	○		Pt		○	○	○	○	○	○		○	○*	○*	○	
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K																																																																																					
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3967	R5000	D0	0																																																																																					
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	1																																																																																					
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S	○	○	○	○	○	○	○	○	○	○	○	○																																																																																						
Pt		○	○	○	○	○	○		○	○*	○*	○																																																																																						
<div><div><div>● When MD=0 and output control “ENU” changes from 0→1, it transmits the ASCII data which starting from S to the communication port 1 (Port1), until reach end of file.</div><div>● S file data can be edited with the programming software PROLADDER or WinProladder (please refer to the explanation of Chapter 14 “ASCII function application”). If necessary the user can also edit the ASCII file directly by change the value of data registers. However, the edited data must be follow the ASCII file format (the details described in chapter 14), otherwise, this instruction will halt the transmission and set the error flag “ERR” to 1. If the entire file is correctly and successfully transmitted, then the output is completed and “DN” is set to 1.</div><div>● The control input of this instruction is of positive edge triggered. Once “ENU” changes from 0→1 then this instruction starts the execution, until finished the transmission of the entire file then the execution is completed. During the transmission, the action flag “ACT” will be kept at 1 all the time. Only when output pause, error, or abort occurs, will it change back to 0.</div><div>● This instruction can be repeatedly used, but only one will be executed (transmit data) at any certain time. It is the obligation of user to make sure the right execution sequence.</div><div>● While this instruction is in execution, if the pause “PAU” is 1, this instruction will pause the transmission of file data. It will resume transmission when the pause “PAU” backs to 0.</div><div>● While this instruction is in execution, if the abort “ABT” is 1, this instruction will abandon the transmission of file data, and then it is able to take next instruction for execution.</div><div>● or detail applications, please refer to Chapter 14 “The Application of ASCII file output function”.</div></div></div>																																																																																																		

FUN 94 ASCWR	ASCII WRITE	FUN 94 ASCWR

- Interface signals:
 - M1927: This signal is control by CPU, it is applied in ASCWR MD:0
 - : ON, it represents that the RTS (connect to the CTS of PLC) of the printer is "False".
I.e. the printer is not ready or abnormal.
 - : OFF, it represents that the RTS of the Printer is "True"; Printer is Ready.

Note: Using the M1927 associates with timer can detect if the printer is abnormal or not.

Slow Up/Slow Down Instructions

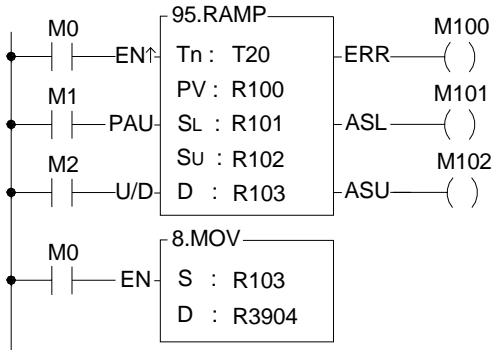
FUN 95 		RAMP FUNCTION FOR D/A OUTPUT												FUN 95 			
RAMP																RAMP	
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FUN 95 **P**
RAMP

RAMP FUNCTION FOR D/A OUTPUT

FUN 95 **P**
RAMP

Program example



Move the ramping value to AO output register R3904

T20: Ramp timer (timer with 0.01 second time base)

R100: preset value of ramp timer (the unit is 0.01 second, 100 for a second).

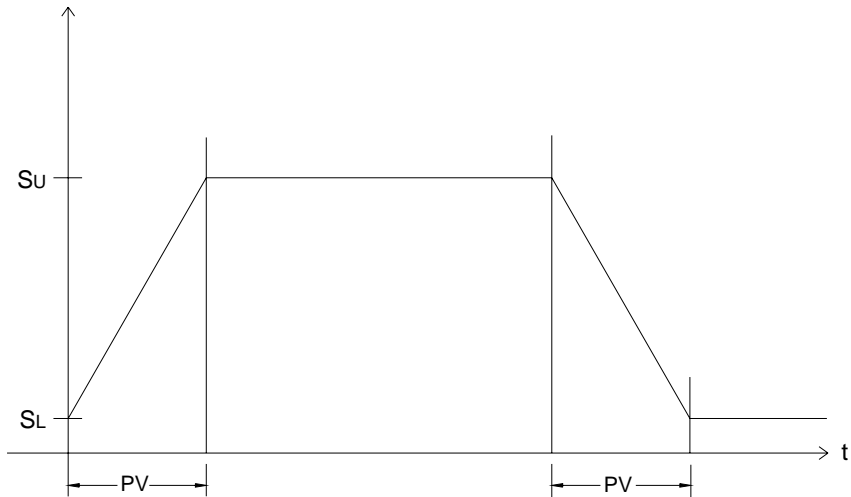
R101: Lower limit value.

R102: Upper limit value.

R103: Register storing current ramp value.

R104: Working register

- If M1974=0, When input control M0 changes from 0→1, it first reset the timer T20 to 0. If M2=1, it will load the R101 (lower limit) value into the R103, and it will increase the output with fixed value $(R102-R101 / R100)$ for every 0.01 second and stores it to register R103. When the T2 timer going up to the preset value R100, the output value equals to R102, and the output M102 will set to 1. If M2=0, will load the R102 (upper limit) value into the R103, and it will decrease the output amount with fixed ratio $(R102-R101 / R100)$ for every 0.01 second and store it to register R103. The T2 timer going up to the preset value R100, the output value equals to R102, and the output M101 will set to 1.
- M1=1, pause the ramping action.
- The value of R102 must be greater than R101, otherwise the ramp action will not be performed, and the output M100 will set to 1.



Slow Up/Slow Down Instruction

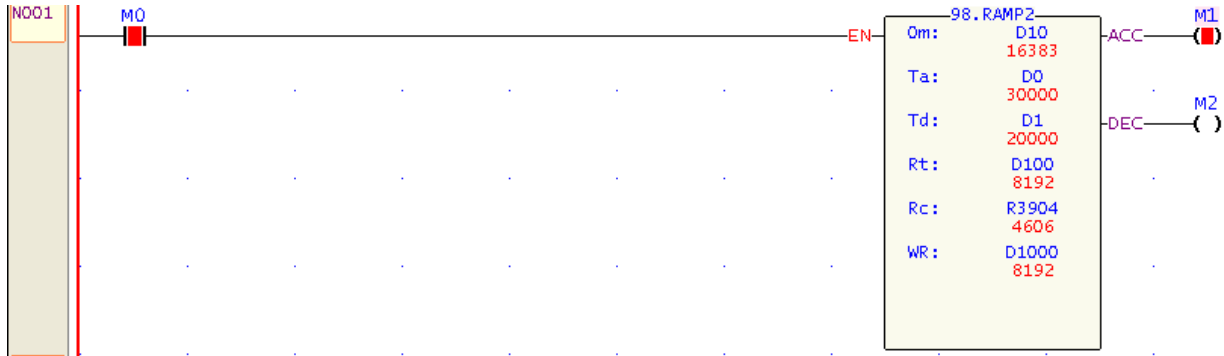
FUN98 RAMP2	TRACKING TYPE RAMP FUNCTION FOR D/A OUTPUT	FUN98 RAMP2																																															
Execution EN	<div><div>98.RAMP2</div><div>Om : Ta : Td : Rt : Rc : WR :</div><div>ACC DEC</div></div>	<p>Om : Maximum output; range from 0~65535</p> <p>Ta : The acceleration time for the output from 0 up to maximum; Range from 0~65000, unit is in mS</p> <p>Td : The deceleration time for the output from maximum down to 0; Range from 0~65000, unit is in mS</p> <p>Rt : Register of target output; Range from 0~65535</p> <p>Rc : Register of current output, it is used for analog output</p> <p>WR : Starting address of working registers, it needs 4 registers</p> <p>* This instruction can be supported in PLC OS firmware V4.60 or late</p>																																															
<table><tr><th rowspan="2">Operand \ Range</th><th>HR</th><th>OR</th><th>ROR</th><th>DR</th><th>K</th></tr><tr><td>R0 R3839</td><td>R3904 R3967</td><td>R5000 R8071</td><td>D0 D3999</td><td>16bit</td></tr><tr><td>Om</td><td>○</td><td>○</td><td>○</td><td>○</td><td>0~65535</td></tr><tr><td>Ta</td><td>○</td><td>○</td><td>○</td><td>○</td><td>0~65000</td></tr><tr><td>Td</td><td>○</td><td>○</td><td>○</td><td>○</td><td>0~65000</td></tr><tr><td>Rt</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td></tr><tr><td>Rc</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td></tr><tr><td>WR</td><td>○</td><td>○</td><td>○*</td><td>○</td><td></td></tr></table>			Operand \ Range	HR	OR	ROR	DR	K	R0 R3839	R3904 R3967	R5000 R8071	D0 D3999	16bit	Om	○	○	○	○	0~65535	Ta	○	○	○	○	0~65000	Td	○	○	○	○	0~65000	Rt	○	○	○	○		Rc	○	○	○	○		WR	○	○	○*	○	
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<ul style="list-style-type: none">● When execution “EN” =0, current output value (Rc) will be 0 immediately; the output indicators ACC=0 and DEC=0.● When execution “EN” =1, this instruction being executed; it will output current value (Rc) first, and then compare the target output value (Rt) with current output value (Rc) every scan; if the target output value is greater than current output value, the current output will be increased according to the rate, which is decided by the settings of acceleration time (Ta) and maximum output (Om), till current output value is equal to the target output value (ACC=1 during this time); if the target output value is less than current output value, the current output will be decreased according to the rate, which is decided by the settings of deceleration time (Td) and maximum output (Om), till current output value is equal to the target output value (DEC=1 during this time).● If the setting value of target output (Rt) is greater than maximum output(Om), the output value will be clamped by the maximum value.● It can have smooth activity for acceleration and deceleration control via the execution of this instruction by using current output value (Rc) for analog output (R39044~R3967).● The setting value of target output (Rt) needs to stay two scan times at least for proper operation.● It needs 4 registers for working, they can not be repeated in use ◦● This instruction is for positive value operation, but it also can have negative output by short and easy application program for help. Please see example 2.																																																	

FUN98
RAMP2

TRACKING TYPE RAMP FUNCTION FOR D/A OUTPUT

FUN98
RAMP2

Example 1 : Positive output for ACC/DEC control



D10 : Setting of maximum output, it is 16383

D0 : The acceleration time for the output from 0 up to maximum, it is 30000mS

D1 : The deceleration time for the output from maximum down to 0, it is 20000mS

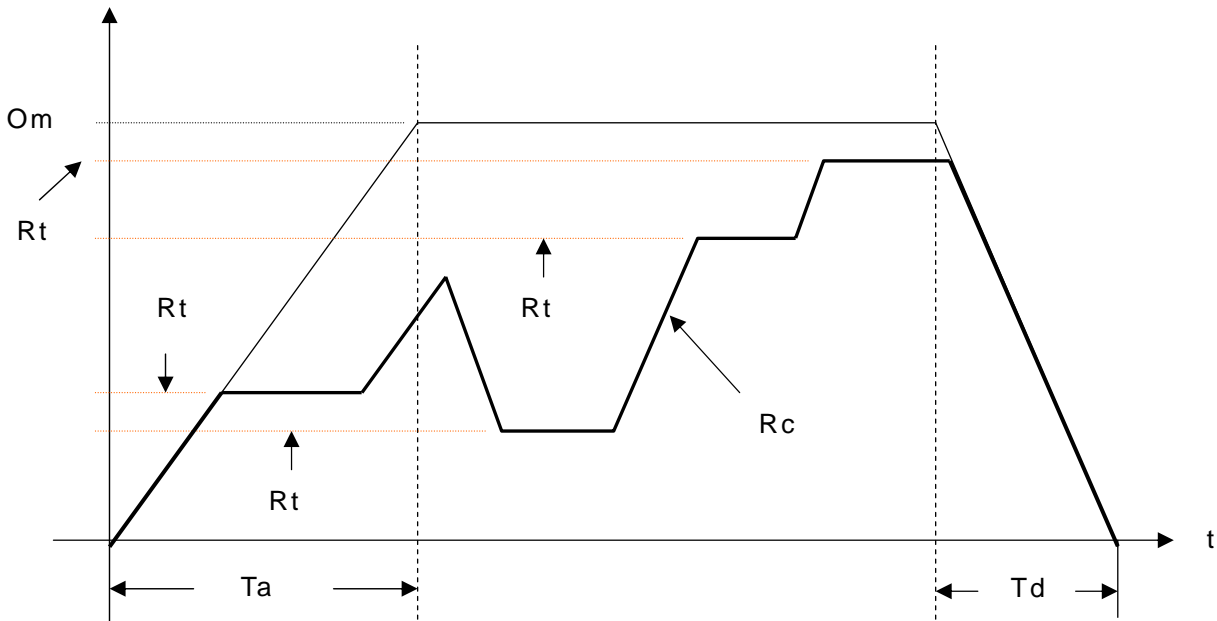
D100 : Setting of target output value, it is 8192

R3904 : Register of current output, it is used for analog output

D1000~D1003 : Working registers

Description: When M0=0, current output value is 0 immediately (No ramp).

When M0=1, it will output the value of R3904 first; and then compare the target output value (D100) with current output value (R3904) every scan; if $D100 > R3904$, the current output value of R3904 will be increased according to the rate of 16383/30000 ($Om=16383, Ta=30000$), till $R3904=D100$ ($ACC=1$ during this time); if $D100 < R3904$, the current output value of R3904 will be decreased according to the rate of 16383/20000 ($Om=16383, Td=20000$), till $R3904=D100$ ($DEC=1$ during this time).



FUN98 RAMP2	TRACKING TYPE RAMP FUNCTION FOR D/A OUTPUT	FUN98 RAMP2
<div>Example 2 : Both positive and negative output for ACC/DEC control</div>		
<p>D10 : Setting of maximum output, it is 8191</p> <p>D0 : The acceleration time for the output from 0 up to maximum, it is 20000mS</p> <p>D1 : The deceleration time for the output from maximum down to 0, it is 10000mS</p> <p>D100 : Setting of target output value, it is 0</p> <p>D200 : Register of current output, it is used for analog output</p> <p>D1000~D1003 : Working registers</p> <p>Description: When M0=0, current output value is 0 immediately (No ramp).</p> <p>When M0=1, it will output the value of D200 first; and then compare the target output value (D100) with current output value (D200) every scan; if $D100 > D200$, the current output value of D200 will be increased according to the rate of 8191/20000 ($Om=8191$, $Ta=20000$), till $D200=D100$ ($ACC=1$ during this time); if $D100 < D200$, the current output value of D200 will be decreased according to the rate of 8191/10000 ($Om=8191$, $Td=10000$), till $D200=D100$ ($DEC=1$ during this time).</p> <p>M100=1, positive output control; M101=1, negative output control.</p> <p>The target output (D100) is always positive value from 0~65535.</p>		

FUN98
RAMP2

TRACKING TYPE RAMP FUNCTION FOR D/A OUTPUT

FUN98
RAMP2

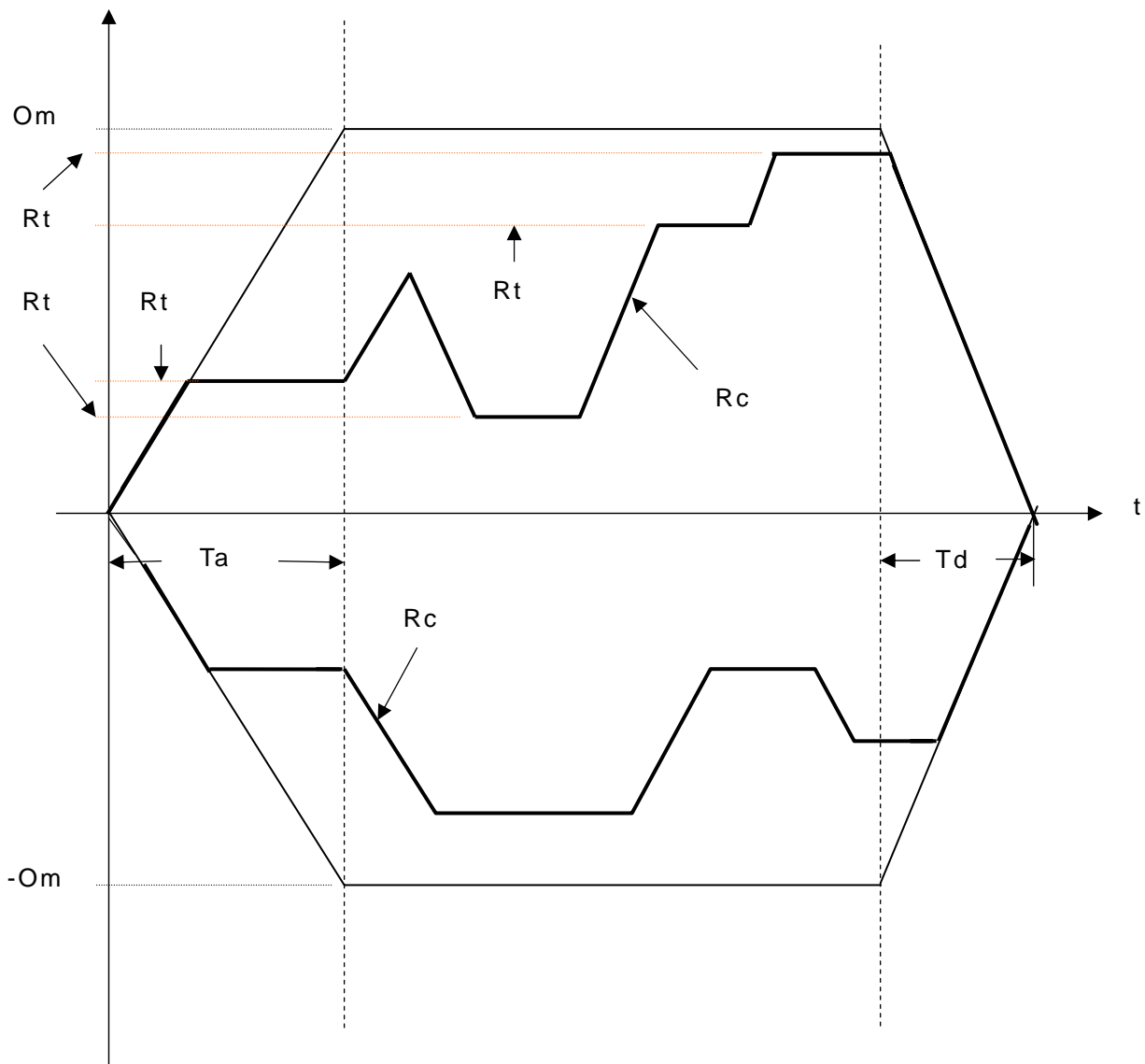
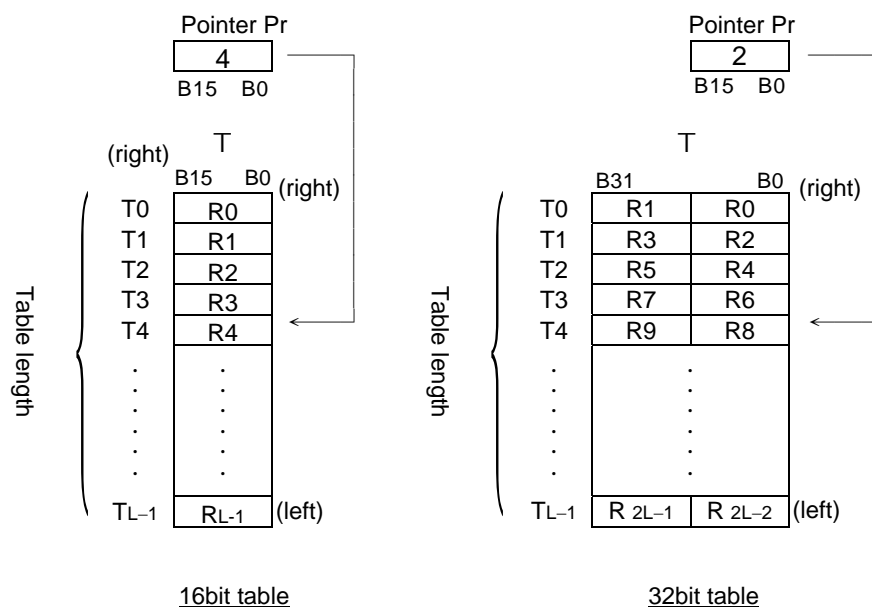


Table Instructions

Fun No.	Mnemonic	Functionality	Fun No.	Mnemonic	Functionality
100	R→T	Register to table data move	107	T_FIL	Table fill
101	T→R	Table to register data move	108	T_SHF	Table shift
102	T→T	Table to table data move	109	T_ROT	Table rotate
103	BT_M	Block table move	110	QUEUE	Queue
104	T_SWP	Block table swap	111	STACK	Stack
105	R-T_S	Register to table search	112	BKCMP	Block compare
106	T-T_C	Table to table compare	113	SORT	Data Sort

- A table consists of 2 or more consecutive registers (16 or 32 bits). The number of registers that comprise the table is called the table length (L). The operation object of the table instructions always takes the register as unit (i.e. 16 or 32 bit data).
- The operation of table instructions are used mostly for data processing such as move, copy, compare, search etc, between tables and registers, or between tables. These instructions are convenient for application.
- Among the table instructions, most instructions use a pointer to specify which register within a table will be the target of operation. The pointer for both 16 and 32-bit table instructions will always be a 16-bit register. The effective range of the pointer is 0 to L-1, which corresponds to registers T₀ to T_{L-1} (a total of L registers). The table shown below is a schematic diagram for 16-bit and 32-bit tables.
- Among the table operations, shift left/right, rotate left/right operations include a movement direction. The direction toward the higher register is called left, while the direction toward the lower register is called right, as shown in the diagram below.



FUN100 D P R→T		REGISTER TO TABLE MOVE												FUN100 D P R→T																																																																																													
		<div><div>Ladder symbol</div><div><div>100DP.R→T</div><div><div>Rs : <div></div></div></div><div><div>Td : <div></div></div></div><div><div>L : <div></div></div></div><div><div>Pr : <div></div></div></div><div><div>END— Move to end</div></div><div><div>ERR— Pointer error</div></div></div></div> <div><div>Rs : Source data , can be constant or register</div><div>Td : Source register for destination table</div><div>L : Length of destination table</div><div>Pr : Pointer register</div><div>Rs, Td can associate with V, Z, P0~P9 index register as indirect addressing</div></div>																																																																																																									
		<table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td>Oper- and</td><td>WX0 WX240</td><td>WY0 WY240</td><td>WM0 WM1896</td><td>WS0 WS984</td><td>T0 T255</td><td>C0 C255</td><td>R0 R3839</td><td>R3840 R3903</td><td>R3904 R3967</td><td>R3968 R4167</td><td>R5000 R8071</td><td>D0 D4095</td><td>16/32bit +/- number</td><td>V · Z P0~P9</td></tr><tr><td>Rs</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td></tr><tr><td>Td</td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td><td>○*</td><td>○*</td><td>○</td><td></td><td>○</td></tr><tr><td>L</td><td></td><td></td><td></td><td></td><td></td><td></td><td>○</td><td></td><td></td><td></td><td>○*</td><td>○</td><td>2~2048</td><td></td></tr><tr><td>Pr</td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td><td>○*</td><td>○*</td><td>○</td><td></td><td></td></tr></table>														Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	Oper- and	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32bit +/- number	V · Z P0~P9	Rs	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Td		○	○	○	○	○	○		○	○*	○*	○		○	L							○				○*	○	2~2048		Pr		○	○	○	○	○	○		○	○*	○*	○				
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR																																																																																													
Oper- and	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32bit +/- number	V · Z P0~P9																																																																																													
Rs	○	○	○	○	○	○	○	○	○	○	○	○	○	○																																																																																													
Td		○	○	○	○	○	○		○	○*	○*	○		○																																																																																													
L							○				○*	○	2~2048																																																																																														
Pr		○	○	○	○	○	○		○	○*	○*	○																																																																																															
		<div><div><div>●</div><div>When move control "EN" = 1 or transition from 0 to 1 (P instruction), the contents of the source register Rs will be written onto the register Tdpr indicated by the pointer Pr within the destination table Td (length is L). Before executing, this instruction will first check the pointer clear "CLR" input signal. If "CLR" is 1, it will first clear the pointer Pr, and then carry out the move operation. After the move has been completed, it will then check the Pr value. If the Pr value has already reached L-1 (point to the last register in the table) then it will only set the move-to-end flag "END" to 1, and finish execution of this instruction. If the Pr value is less than L-1, then it must again check the pointer increment "INC" input signal. If "INC" is 1, then Pr value will be also increased. Besides, pointer clear "CLR" is able to operate independently, without being influenced by other input.</div></div><div><div>●</div><div>The effective range of the pointer is 0 to L-1. Beyond this range, the pointer error "ERR" will be set to 1, and this instruction will not be performed.</div></div></div> <div><div><div><div>X1</div><div>— EN</div><div>— INC</div><div>— CLR</div></div><div><div>100P.R→T</div><div><div>Rs : R 0</div><div>Td : R 10</div><div>L : 8</div><div>Pr : R 50</div></div><div><div>END—</div><div>ERR—</div></div></div></div><div><div><div>Pr</div><div>4 R50</div><div>Td</div><div><div>0000 R10(T0)</div><div>0000 R11(T1)</div><div>0000 R12(T2)</div><div>0000 R13(T3)</div><div>0000 R14(T4)</div><div>0000 R15(T5)</div><div>0000 R16(T6)</div><div>0000 R17(T7)</div></div><div><div>Rs</div><div>8888 R0</div></div><div>Before</div></div><div><div><div>X0 = 1</div><div>(First)</div></div><div><div>Pr</div><div>5 R50</div><div>Td</div><div><div>0000 R10</div><div>0000 R11</div><div>0000 R12</div><div>0000 R13</div><div>8888 R14</div><div>0000 R15</div><div>0000 R16</div><div>0000 R17</div></div><div>First time result</div></div><div><div><div>X0 = 1</div><div>(Second)</div></div><div><div>Pr</div><div>6 R50</div><div>Td</div><div><div>0000 R10</div><div>0000 R11</div><div>0000 R12</div><div>0000 R13</div><div>8888 R14</div><div>8888 R15</div><div>0000 R16</div><div>0000 R17</div></div><div>Second time result</div></div></div></div></div></div>																																																																																																									

Table Instructions

FUN101 D P T→R		TABLE TO REGISTER MOVE														FUN101 D P T→R																																																																																										
		<div><div>Ladder symbol</div><div>101DP.T→R</div><div>Move control—EN Ts : <div></div>—END— Move to end L : <div></div> Pointer increment—INC Pr : <div></div>—ERR— Pointer error Rd : <div></div> Pointer clear—CLR</div></div>														Ts : Source table starting register L : Length of source table Pr : Pointer register Rd : Destination register Ts, Rd may combine with V, Z, P0~P9 to serve indirect address application																																																																																										
		<table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td rowspan="2">Ope- rand</td><td>WX0 WX240</td><td>WY0 WY240</td><td>WM0 WM1896</td><td>WS0 WS984</td><td>T0 T255</td><td>C0 C255</td><td>R0 R3839</td><td>R3840 R3903</td><td>R3904 R3967</td><td>R3968 R4167</td><td>R5000 R8071</td><td>D0 D4095</td><td>16/32bit +/- number</td><td>V · Z P0~P9</td></tr><tr><td>Ts</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td></tr><tr><td>L</td><td></td><td></td><td></td><td></td><td></td><td></td><td>○</td><td></td><td></td><td></td><td>○*</td><td>○</td><td></td><td></td></tr><tr><td>Pr</td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td><td>○*</td><td>○*</td><td>○</td><td>2~2048</td><td></td></tr><tr><td>Rd</td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td><td>○*</td><td>○*</td><td>○</td><td></td><td>○</td></tr></table>														Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32bit +/- number	V · Z P0~P9	Ts	○	○	○	○	○	○	○	○	○	○	○		○	L							○				○*	○			Pr		○	○	○	○	○	○		○	○*	○*	○	2~2048		Rd		○	○	○	○	○	○		○	○*	○*	○		○		
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR																																																																																												
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32bit +/- number	V · Z P0~P9																																																																																												
	Ts	○	○	○	○	○	○	○	○	○	○	○		○																																																																																												
L							○				○*	○																																																																																														
Pr		○	○	○	○	○	○		○	○*	○*	○	2~2048																																																																																													
Rd		○	○	○	○	○	○		○	○*	○*	○		○																																																																																												
<ul style="list-style-type: none">When move control "EN" = 1 or transition from 0 to 1 (P instruction), the value of the register Tspr specified by pointer Pr within source table Ts (length is L) will be written into the destination register Rd. Before executing, this instruction will first check the input signal of pointer clear "CLR". If "CLR" is 1, it will first clear Pr and then carry out the move operation. After completing the move operation, it will then check the value of Pr. If the Pr value has already reached L-1 (point to the last register in the table), then it sets the move-to-end flag to 1, and finishes executing of this instruction. If Pr is less than L-1, it check the status of "INC". If "INC" is 1, then it will increase Pr and finish the execution of this instruction. Besides, pointer clear "CLR" can execute independently and is not influenced by other inputs.The effective range of the pointer is 0 to L-1. Beyond this range the pointer error "ERR" will be set to 1 and this instruction will not be carried out.																																																																																																										
<div><div><div>X0</div><div>— —EN</div><div>—INC</div><div>—CLR</div></div><div>101P.T→R</div><div>Ts : R 0—END— L : 9 Pr : R 19—ERR— Rd : R 20</div></div>																<ul style="list-style-type: none">In the example at left, at the very beginning Pr = 7 and Ts and Rd are as shown at left in the diagram below. When X0 have a transition from 0→1 twice, the results are shown at right in the diagram below.At the second time execution, the pointer has already reached to the end so there will be no increment.																																																																																										
<div><div><div><div>Ts</div><div><div>R0(T0)</div><div>1 1 1 1</div></div><div><div>R1(T1)</div><div>2 2 2 2</div></div><div><div>R2(T2)</div><div>3 3 3 3</div></div><div><div>R3(T3)</div><div>4 4 4 4</div></div><div><div>R4(T4)</div><div>5 5 5 5</div></div><div><div>R5(T5)</div><div>6 6 6 6</div></div><div><div>R6(T6)</div><div>7 7 7 7</div></div><div><div>R7(T7)</div><div>8 8 8 8</div></div><div><div>R8(T8)</div><div>9 9 9 9</div></div></div><div><div>Pr</div><div><div>7</div><div>R19</div></div></div><div><div>Rd</div><div><div>0000</div><div>R20</div></div></div><div><div>END</div><div><div>0</div></div></div></div><div>Before execution</div><div><div><div>X0=</div><div>↑</div><div>(first)</div><div>⇒</div></div><div><div>Pr</div><div><div>8</div><div>R19</div></div></div><div><div>Rd</div><div><div>8 8 8 8</div><div>R20</div></div></div><div><div>END</div><div><div>0</div></div></div></div><div>First time execution</div><div><div><div>X0=</div><div>↑</div><div>(second)</div><div>⇒</div></div><div><div>Pr</div><div><div>8</div><div>R19</div></div></div><div><div>Rd</div><div><div>9 9 9 9</div><div>R20</div></div></div><div><div>END</div><div><div>1</div></div></div></div><div>Second time execution</div></div>																																																																																																										





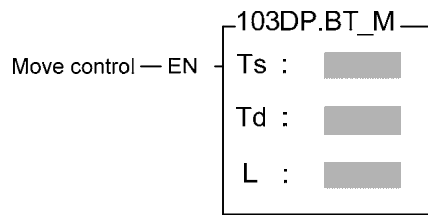
FUN102 D P T→T		TABLE TO TABLE MOVE														FUN102 D P T→T	
		Ladder symbol															
		102DP.T→T															
Move control—EN		Ts :  END— Move to end															
		Td : 															
Pointer increment—INC		L :  ERR— Pointer error															
Pointer clear—CLR		Pr : 															
		Ts : Starting number of source table register Td : Starting number of destination table register L : Table (Ts and Td) length Pr : Pointer register Ts, Td may combine with V, Z, P0~P9 to serve indirect address application															

Table Instructions

FUN103 D P BT_M	BLOCK TABLE MOVE	FUN103 D P BT_M
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Ladder symbol



Ts : Starting register for source table

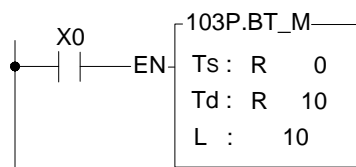
Td : Starting register for destination table

L: Lengths of source and destination tables

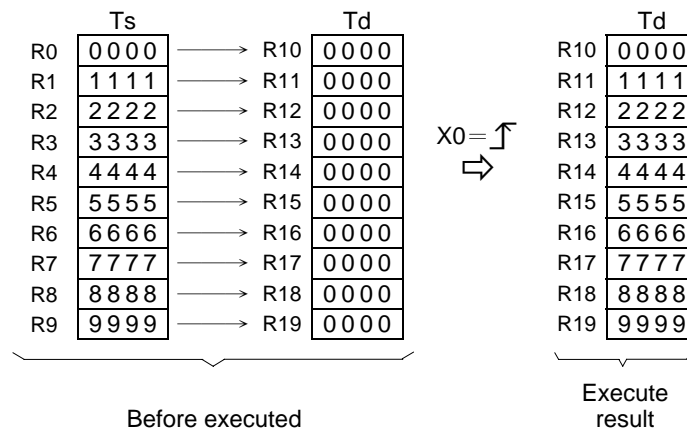
Ts, Td may combine with V, Z, P0~P9 to serve indirect

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	2	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	256	P0~P9
Ts	○	○	○	○	○	○	○	○	○	○	○	○		○
Td		○	○	○	○	○	○		○	○*	○*	○		○
L							○				○*	○	○	

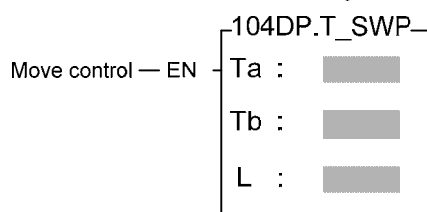
- In this instruction the source table and destination table are the same length. When this instruction was executed all the data in the Ts table is completely copied to Td. No pointer is involved in this instruction.
- When move control "EN" = 1 or have a transition from 0 to 1 (**P** instruction), all the data from source table Ts (length L) is copied to the destination table Td, which is the same length.
- One table is completely copied every time this instruction is executed, so if the table length is long, it will be very time consuming. In practice, P modifier should be used to avoid time waste caused by each scan repeating the same movement action.



- The diagram at left below is the status before execution. When X0 from 0→1, the content of R0~R9 in Ts table will copy to R10~R19.



FUN104 D P T_SWP	BLOCK TABLE SWAP	FUN104 D P T_SWP
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Ladder symbol

Ta : Starting register of Table a

Tb : Starting register of Table b

L : Lengths of Table a and b

Ts, Td may combine with V, Z, P0~P9 to serve indirect address application

Range	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	K	XR
Ope- rand	WY0	WM0	WS0	T0	C0	R0	R3904	R3968	R5000	D0	2	V · Z
	WY240	WM1896	WS984	T255	C255	R3839	R3967	R4167	R8071	D4095	256	P0~P9
Ta	○	○	○	○	○	○	○	○*	○*	○		○
Tb	○	○	○	○	○	○	○	○*	○*	○		○
L						○			○*	○	○	

- This instruction swaps the contents of Tables a and b, so the table must be the same length, and the registers in the table must of write able. Since a complete swap is done with each time the instruction is executed, no pointer is needed.
- When move control "EN" = 1 or have a transition from 0 to 1 (**P** instruction), the contents of Table a and Table b will be completely swapped.
- This instruction will swap all the registers specified in L each time the instruction is executed, so if the table length is big, it will be very time consuming, therefore P instruction should be used.

- The diagram at left below is the status before execution.
When X0 from 0→1, the contents of R0~R9 in Ts table will swap with R10~R19.

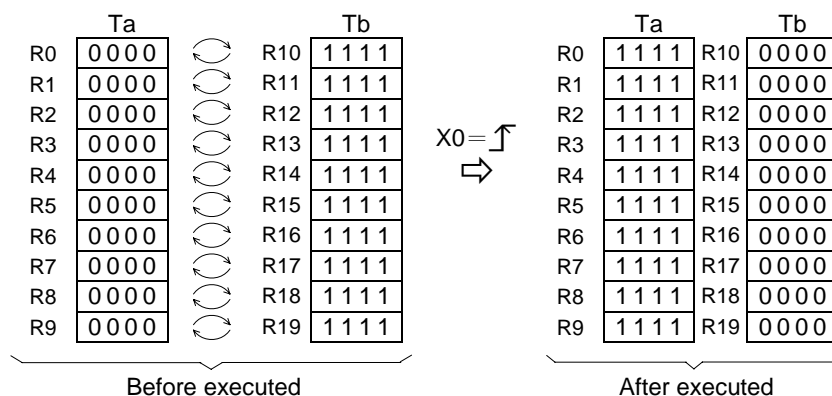
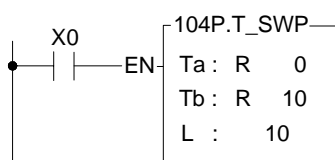














Table Instructions

FUN105  		REGISTER TO TABLE SEARCH												FUN105  																																																																																																						
R-T_S														R-T_S																																																																																																						
<div><div><div><div>Ladder symbol</div><div><div>105DP.R-T_S</div><div><div>Search control — EN</div><div>Search from head — FHD</div><div>Different/same option — D/S</div></div><div><div>Rs : </div><div>Ts : </div><div>L : </div><div>Pr : </div></div><div><div>FND — Found objective</div><div>END — Search to end</div><div>ERR — Pointer error</div></div></div></div></div><div><div>Rs : Data to search, It can be a constant or a register</div><div>Ts : Starting register of table being searched</div><div>L : Label length</div><div>Pr : Pointer of table</div><div>Rs, Ts may combine with V, Z, P0~P9 to serve indirect address application</div></div></div>																																																																																																																				
<table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td rowspan="2">Oper- and</td><td>WX0</td><td>WY0</td><td>WM0</td><td>WS0</td><td>T0</td><td>C0</td><td>R0</td><td>R3840</td><td>R3904</td><td>R3968</td><td>R5000</td><td>D0</td><td rowspan="2">16/32-bit +/- number</td><td rowspan="2">V · Z</td></tr><tr><td>WX240</td><td>WY240</td><td>WM1896</td><td>WS984</td><td>T255</td><td>C255</td><td>R3839</td><td>R3903</td><td>R3967</td><td>R4167</td><td>R8071</td><td>D4095</td><td>P0~P9</td></tr><tr><td>Rs</td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td></tr><tr><td>Ts</td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td></tr><tr><td>L</td><td></td><td></td><td></td><td></td><td></td><td></td><td><input type="checkbox"/></td><td></td><td></td><td></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td>2~256</td><td></td></tr><tr><td>Pr</td><td></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td></td><td></td></tr></table>		Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	Oper- and	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	16/32-bit +/- number	V · Z	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	P0~P9	Rs	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ts	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	L							<input type="checkbox"/>				<input type="checkbox"/>	<input type="checkbox"/>	2~256		Pr		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>														
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR																																																																																																						
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	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095			P0~P9																																																																																																					
Rs	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>																																																																																																						
Ts	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>																																																																																																						
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Pr		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>																																																																																																								
<div><div><div><div>● When search control "EN" = 1 or has a transition from 0 to 1 ( instruction), will search from the first register of Table Ts (when "FHD" = 1 or Pr value has reached L-1), or from the next register (Tspr + 1) pointed by the pointer within the table ("FHD" = 0, while Pr value is less than L-1) to find the first data different with Rs(when D/S = 1) or find the first data the same with Rs (when D/S = 0). If it find a data match the condition it will immediately stop the search action, and the pointer Pr will point to that data and found objective flag "FND" will set to 1. When the searching has searched to the last register of the table, the execution of the instruction will stop, whether it was found or not. In that case the search-to-end flag "END" will be set to 1 and the Pr value will stop at L-1. When this instruction next time is executed, Pr will automatically return to the head of the table (Pr = 0) before the search begin.</div><div>● The effective range of Pr is 0 to L-1. If the value exceeds this range then the pointer error flag "ERR" will change to 1, and this instruction will not be carried out.</div></div></div><div><div><div><div><div>X0</div><div>EN</div><div>—FHD</div><div>—D/S</div></div><div><div>105P.R-T_S</div><div>Rs : 5555</div><div>Ts : R 0</div><div>L : 10</div><div>Pr : R 20</div></div><div><div>FND—</div><div>END—</div><div>ERR—</div></div></div></div><div><div>● The instruction at left is searching the table for a register with the value 5555 (because D/S = 0, it is searching for same value). Before execution, the pointer point to R2, but the starting point of the search is Pr + 1 (i.e. it starts from R3). After X0 has transition from 0→1 3 times, the results of each search may be obtained as shown in the diagram below.</div></div></div><div><div><div><div><div>Pr</div><div>R20 2</div><div>Rs</div><div>5555</div></div><div><div>Ts</div><div>R0 5555</div><div>R1 0000</div><div>R2 5555</div><div>R3 2222</div><div>R4 3333</div><div>R5 4444</div><div>R6 5555</div><div>R7 6666</div><div>R8 7777</div><div>R9 8888</div></div><div>Before execution</div></div></div><div><div><div><div><div>① X0 = </div><div>(First)</div><div>Pr</div><div>R20 6</div><div>FN</div><div>1</div><div>EN</div><div>0</div></div><div><div>② X0 = </div><div>(Second)</div><div>Pr</div><div>R20 9</div><div>FN</div><div>0</div><div>EN</div><div>1</div></div><div><div>③ X0 = </div><div>(Third)</div><div>Pr</div><div>R20 0</div><div>FN</div><div>1</div><div>EN</div><div>0</div></div><div>After execution</div></div></div></div></div></div>																																																																																																																				

FUN106 D P T-T_C	TABLE TO TABLE COMPARE	FUN106 D P T-T_C
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Ladder symbol

Compare control — EN

Compare from head — FHD

Different/Same option — D/S

106DP.T-T_C

Ta :

Tb :

L :

Pr :

FND — Found objective

END — Compare to end

ERR — Pointer error

Ta : Starting register of Table a

Tb : Starting register of Table b

L : Lengths of Table

Pr : Pointer

Ta, Tb may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	2	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	256	P0~P9
Ta	○	○	○	○	○	○	○	○	○	○	○	○	○	○
Tb	○	○	○	○	○	○	○	○	○	○	○	○	○	○
L							○				○*	○	○	
Pr		○	○	○	○	○	○		○	○*	○*	○		

- When comparison control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), then starting from the first register in the tables Ta and Tb (when "FHD" = 1 or Pr value has reached L-1) or starting from the next pair of registers (Tapr+1 and Tbpr+1) pointed by Pr ("FHD" = 0, while Pr is less than L-1), this instruction will search for pairs of registers with different values (when "D/S" = 1) or the same value (when "D/S" = 0). When search found (either different or the same), it will immediately stop the search and the pointer Pr will point to the register pairs met the search criteria. The found flag "FND" will be set to 1. When it has searched to the last register of the table, the instruction will stop executing. whether it found or not. The compare-to-end flag "END" will be set to 1, and the pointer value will stop at L-1. When this instruction is executed next time, Pr will automatically return to the head of the table to begin the search. The effective range of Pr is 0 to L-1. The Pr value should not changed by other programs during the operation. As this will affect the result of the search. If the Pr value not in the effective range, the pointer error flag "ERR" will be set to 1, and this instruction will not be carried out.
- The instruction at left starts from the register next to the register pointed by the pointer (because "FHD" is 0) to search for register pairs with different data (because "D/S" is 1) within the 2 tables. At the very beginning, Pr points to Ta1 and Tb1. There are 3 different pairs of data at the position 1,3,6 of the table. However, it does not compare from the beginning, and this instruction will start searching from position 3 downwards. After X0 has changed 3 times from 0 to 1, the results are shown in the diagram below.

① X0 = (First)

② X0 = (Second)

③ X0 = (Third)

Pr

R10 1

Ta				Tb			
R0	0	0	0	R11	0	0	0
R1	1	1	1	R12	0	0	0
R2	2	2	2	R13	2	2	2
R3	3	3	3	R14	1	2	3
R4	4	4	4	R15	4	4	4
R5	5	5	5	R16	5	5	5
R6	6	6	6	R17	0	0	0
R7	7	7	7	R18	7	7	7
R8	8	8	8	R19	8	8	8
R9	9	9	9	R20	9	9	9

Before execution

Pr

R10 3

FN 1 EN 0

Pr

R10 6

FN 1 EN 0

Pr

R10 9

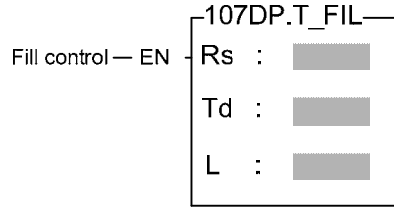
FN 0 EN 1

After execution

Table Instructions

FUN107 D P T_FIL	TABLE FILL	FUN107 D P T_FIL
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Ladder symbol



Rs : Source data to fill, can be a constant or a register

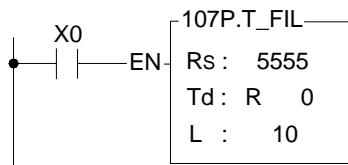
Td : Starting register of destination table

L :Table length

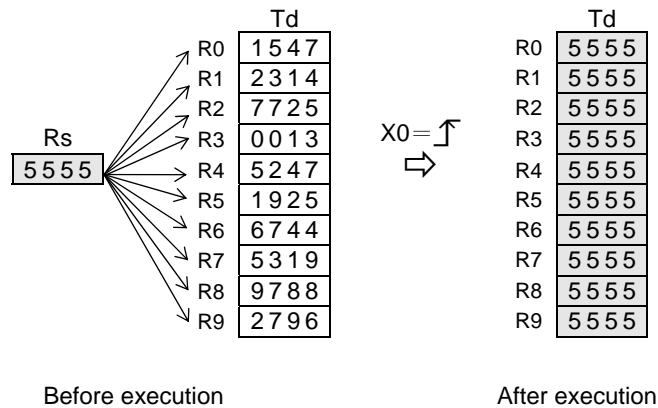
Rs, Td may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number	V、Z P0~P9
Ts	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Td	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
L	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	2~256	<input type="radio"/>

- When fill control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), the Rs data will be filled into all the registers of the table Td.
- This instruction is mainly used for clearing the table (fill 0) or unifying the table (filling in the same values). It should be used with the P instruction.



- The instruction at left will fill 5555 into the whole table Td. The results are as shown in the diagram below.



FUN108 D P T_SHF	TABLE SHIFT	FUN108 D P T_SHF
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Ladder symbol

Shift control — EN

Left/Right direction — L/R

108DP.T_SF

IW :

Ts :

Td :

L :

OW :

IW : Data to fill the room after shift operation, can be a constant or a register

Ts : Source table

Td : Destination table storing shift results

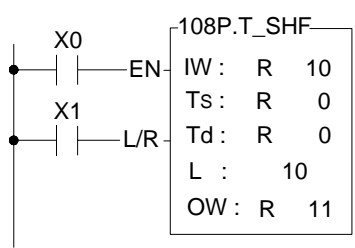
L : Lengths of tables Ts and Td

OW : Register to accept the shifted out data

Ts, Td may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Operand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number	V、Z P0~P0
IW	○	○	○	○	○	○	○	○	○	○	○	○	○	
Ts	○	○	○	○	○	○	○	○	○	○	○	○	○	○
Td		○	○	○	○	○	○		○	○*	○*	○		○
L							○				○*	○	2~256	
OW		○	○	○	○	○	○		○	○*	○*	○		

- When shift control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), all the data from table Ts will be taken out and shifted one position to the left (when "L/R" = 1) or to the right (when "L/R" = 0). The room created by the shift operation will be filled by IW and the results will be written into table Td. The data shifted out will be written into OW.



- In the program at left, Ts and Td is the same table. Therefore, the table shifts itself and then writes back to itself (the table must be writ able). It first perform a shift left operation (let X1 = 1, and X0 go from 0→1) then perform a shift to right operation (let X1 = 0, and makes X0 go from 0→1). The result are shown at right in the diagram below.

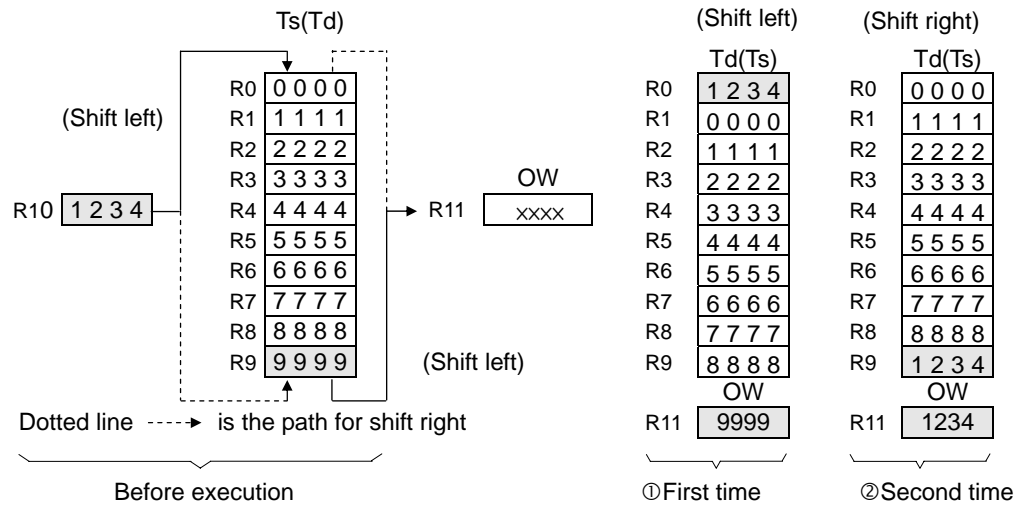


Table Instructions

FUN109 **D P**
T_ROT

TABLE ROTATE

FUN109 **D P**
T_ROT

Ladder symbol

109DP.T_ROT

Rotate control — EN
Ts :

Left/Right direction — L/R
Td :

L :

Ts : Source table for rotate

Td : Destination table storing results of rotation

L : Lengths of table

Ts, Td may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	2	V · Z
Oper- and	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	256	P0~P9
Ts	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>
Td		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input checked="" type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>		<input type="radio"/>
L							<input type="radio"/>				<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	

- When rotation control "EN" = 1 or has a transition from 0 to 1(**P** instruction), the data from the table of Ts will be rotated 1 position to the left (when "L/R" = 1) or 1 position to the right (when "L/R" = 0). The results of the rotation will then be written onto table Td.

X0

X1

109P.T_ROT

EN
Ts : R 0

L/R
Td : R 0

L : 10

- In the program at left, Ts and Td is the same table. The table after rotation will write back to itself. It first perform one left rotation (let X1 = 1, and X0 go from 0→1), and then performs one right rotation (let X1 = 0, and X0 go from 0→1). The results are shown at right in the diagram below.

Rotate left Rotate right

Ts(Td)

R0	0 0 0 0	(right)
R1	1 1 1 1	
R2	2 2 2 2	
R3	3 3 3 3	
R4	4 4 4 4	
R5	5 5 5 5	
R6	6 6 6 6	
R7	7 7 7 7	
R8	8 8 8 8	
R9	9 9 9 9	(left)

Before execution

(Rotate left)

Td(Ts)

R0	9 9 9 9
R1	0 0 0 0
R2	1 1 1 1
R3	2 2 2 2
R4	3 3 3 3
R5	4 4 4 4
R6	5 5 5 5
R7	6 6 6 6
R8	7 7 7 7
R9	8 8 8 8

①First time

(Rotate right)

Td(Ts)

R0	0 0 0 0
R1	1 1 1 1
R2	2 2 2 2
R3	3 3 3 3
R4	4 4 4 4
R5	5 5 5 5
R6	6 6 6 6
R7	7 7 7 7
R8	8 8 8 8
R9	9 9 9 9

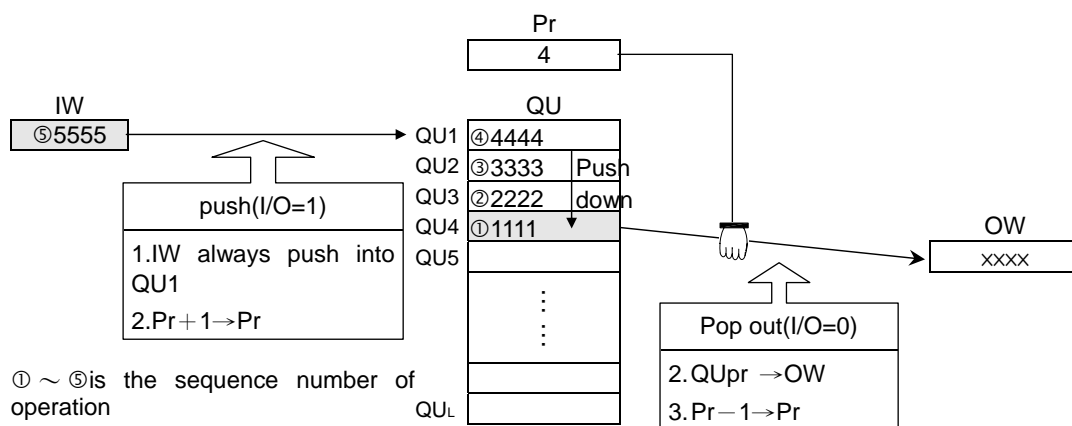
②Second time

FUN110 D P QUEUE	QUEUE	FUN110 D P QUEUE
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Ladder symbol		IW : Data pushed into queue, can be a constant or a register	
Execution control — EN	110DP.QUEUE	EPT — Queue empty FUL — Queue ERR — Pointer error	QU : Starting register of queue L : Size of queue Pr : Pointer register OW : Register accepting data popped out from queue QU may combine with V, Z, P0~P9 to serve indirect address application
	IW :		
	QU :		
	L :		
	Pr :		
In/Out control — I/O	OW :		



Range Ope- rand	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number	V · Z P0~P9
IW	○	○	○	○	○	○	○	○	○	○	○	○	○	
QU		○	○	○	○	○	○		○	○	○*	○		○
L							○				○*	○	2~256	
Pr		○	○	○	○	○	○		○	○*	○*	○		
OW		○	○	○	○	○	○		○	○*	○*	○		

- Queue is also a kind of table. It is different from ordinary table in that its queue register numbers go from 1 to L and not from 0 to L-1. In other words QU₁~QU_L respectively correspond to pointers Pr = 1 to L, and Pr = 0 is used to show that the queue is empty.
- Queue is a first in first out (FIFO) device, i.e. - the data that first pushed into the queue will be the first to pop out from the queue. A queue is comprised of L consecutive 16 or 32 bit registers (**D** instruction) starting from the QU register, as in the diagram below:

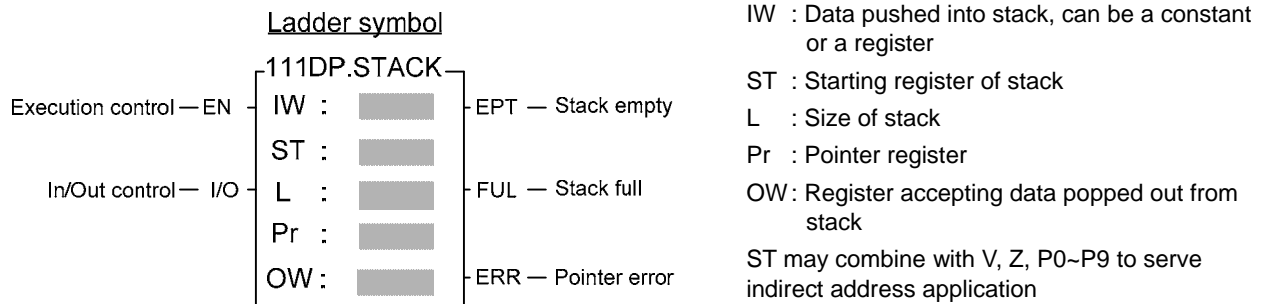


- When execution control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), the status of in/out control "I/O" determines whether the IW data will be pushed into the queue (when "I/O" = 1) or be popped out and transferred to OW (when "I/O" = 0). As shown in the diagram above, the IW data will always be pushed into the first (QU₁) register of the queue. After it has been pushed in, Pr will immediately be increased by 1, so that the pointer can always point to the first data that was pushed into the queue. When it is popped out, the data pointed by Pr will be transferred directly to OW. Pr will be reduced by 1, so that it still point to the first data remained in the queue.

Table Instructions

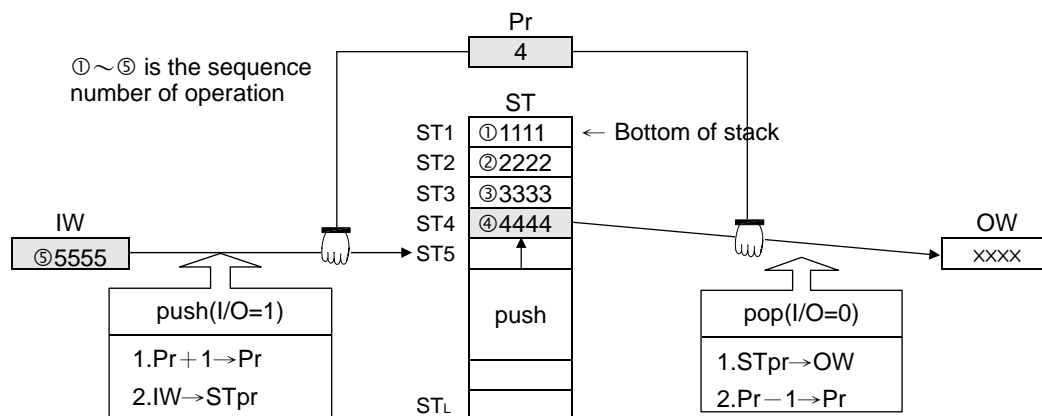
FUN110  QUEUE	QUEUE	FUN110  QUEUE
<div><div><div><div><div>X0</div><div>X1</div></div><div><div>EN</div><div>I/O</div></div></div><div><div><div>110P.QUEUE</div><div>IW : R 0</div><div>QU : R 2</div><div>L : 10</div><div>Pr : R 1</div><div>OW : R 20</div></div><div><div>EPT—</div><div>FUL—</div><div>ERR—</div></div></div></div></div>		
<div><div><div><div><div>Pr</div><div>5</div></div><div><div>QU</div><div><div><div>QU1</div><div>5555</div><div>R2</div></div><div><div>QU2</div><div>4444</div><div>R3</div></div><div><div>QU3</div><div>3333</div><div>R4</div></div><div><div>QU4</div><div>2222</div><div>R5</div></div><div><div>QU5</div><div>1111</div><div>R6</div></div><div><div>QU6</div><div></div><div>R7</div></div><div><div>QU7</div><div></div><div>R8</div></div><div><div>QU8</div><div></div><div>R9</div></div><div><div>QU9</div><div></div><div>R10</div></div><div><div>QU10</div><div></div><div>R11</div></div></div></div><div><div><div>OW</div><div>xxxx</div><div>R20</div></div><div><div>↑</div><div>OW unchanged</div></div></div></div><div>After push in (X1=1 , X0 from 0→1)</div></div><div><div><div><div><div>Pr</div><div>4</div></div><div><div>QU</div><div><div><div>QU1</div><div>5555</div><div>R2</div></div><div><div>QU2</div><div>4444</div><div>R3</div></div><div><div>QU3</div><div>3333</div><div>R4</div></div><div><div>QU4</div><div>2222</div><div>R5</div></div><div><div>QU5</div><div></div><div>R6</div></div><div><div>QU6</div><div></div><div>R7</div></div><div><div>QU7</div><div></div><div>R8</div></div><div><div>QU8</div><div></div><div>R9</div></div><div><div>QU9</div><div></div><div>R10</div></div><div><div>QU10</div><div></div><div>R11</div></div></div></div><div><div><div>OW</div><div>1111</div><div>R20</div></div></div></div><div>After pop off (X1=0 , X0 from 0→1)</div></div></div></div>		

FUN111 D P STACK	STACK	FUN111 D P STACK
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Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Operand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number	V · Z P0~P9
IW	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	
ST		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>
L							<input type="radio"/>				<input type="radio"/>	<input type="radio"/>	2~256	
Pr		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		
OW		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		

- Like queue, stack is also a kind of table. The nature of its pointer is exactly the same as with queue, i.e. $Pr = 1$ to L , which corresponds to ST_1 to ST_L , and when $Pr = 0$ the stack is empty.
- Stack is the opposite of queue, being a last in first out (LIFO) device. This means that the data that was most recently pushed into the stack will be the first to be popped out of the stack. The stack is comprised of L consecutive 16 or 32-bit (**D** instruction) registers starting from ST , as shown in the following diagram:



- When execution control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), the status of in/out control "I/O" determines whether the IW data will be pushed into the stack (when "I/O" = 1), or the data pointed by Pr within the stack (the data most recently pushed into the stack) will be moved out and transferred to OW (when "I/O" = 0). Note that the data pushed in is stacking, so before pushed in, Pr will increased by 1 to point to the top of the stack then the data will be pushed in. When it is popped out, the data pointed by pointer Pr (the most recently pushed in data) will be transferred to OW. After then Pr will decreased by 1. Under any circumstances, the pointer Pr will always point to the data that was pushed into the stack most recently.





Table Instructions

FUN111   STACK	STACK	FUN111   STACK
<div><div><div><div><div>X0</div><div>EN</div></div><div>X1</div><div>I/O</div></div><div><div>111P.STACK</div><div>IW : R 0</div><div>ST : R 2</div><div>L : 10</div><div>Pr : R 1</div><div>OW : R 20</div></div><div><div>EPT</div><div>FUL</div><div>ERR</div></div></div></div> <div><div><div><div><div>●</div><div>When no data has yet been pushed into the stack or the pushed in data has already been popped out (Pr = 0), the stack empty flag "EPT" will set to 1. In this case any further pop up actions, will be ignored. If more data is pushed than popped out, sooner or latter the stack will be full (pointer Pr points to ST_L position), and the stack full flag "FUL" will set to 1. In this case any further push actions, will be ignored. As with queue, the stack pointer in normal case should not be changed by other instructions. If there is a special application which requires to set the Pr value, then its effective range is 0 to L (0 means empty, 1 to L respectively correspond to ST₁ to ST_L). Beyond this range, the pointer error flag "ERR" will set to 1, and the instruction will not be carried out.</div></div></div></div><div><div><div><div><div>●</div><div>The program at left assumes that the initial content of the stack is just as in the diagram of a stack on the preceding page. The operation illustrated in this example is to push a data and than pop it from stack. The results are shown below. Under any circumstances, Pr always point to the data that was most recently pushed into the stack.</div></div></div></div><div><div><div><div><div><div><div>Pr</div><div>5</div><div>R1</div></div><div><div>ST</div><div><div>ST1</div><div>1111</div><div>R2</div></div><div><div>ST2</div><div>2222</div><div>R3</div></div><div><div>ST3</div><div>3333</div><div>R4</div></div><div><div>ST4</div><div>4444</div><div>R5</div></div><div><div>ST5</div><div>5555</div><div>R6</div></div><div><div>ST6</div><div></div><div>R7</div></div><div><div>ST7</div><div></div><div>R8</div></div><div><div>ST8</div><div></div><div>R9</div></div><div><div>ST9</div><div></div><div>R10</div></div><div><div>ST10</div><div></div><div>R11</div></div></div></div><div><div><div>OW</div><div>xxxx</div><div>R20</div></div><div>↑</div><div>OW unchanged</div></div></div><div>After push(X1=1 , X0 from 0→1)</div></div><div><div><div><div><div><div><div>Pr</div><div>4</div><div></div></div><div><div>QU</div><div><div>ST1</div><div>1111</div><div>R2</div></div><div><div>ST2</div><div>2222</div><div>R3</div></div><div><div>ST3</div><div>3333</div><div>R4</div></div><div><div>ST4</div><div>4444</div><div>R5</div></div><div><div>ST5</div><div></div><div>R6</div></div><div><div>ST6</div><div></div><div>R7</div></div><div><div>ST7</div><div></div><div>R8</div></div><div><div>ST8</div><div></div><div>R9</div></div><div><div>ST9</div><div></div><div>R10</div></div><div><div>ST10</div><div></div><div>R11</div></div></div></div><div><div><div>OW</div><div>5555</div><div>R20</div></div></div><div>After pop up(X1=0 , X0 from 0→1)</div></div></div></div></div></div></div></div></div>		

FUN112 D P BKCMP	BLOCK COMPARE (DRUM)	FUN112 D P BKCMP
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Ladder symbol

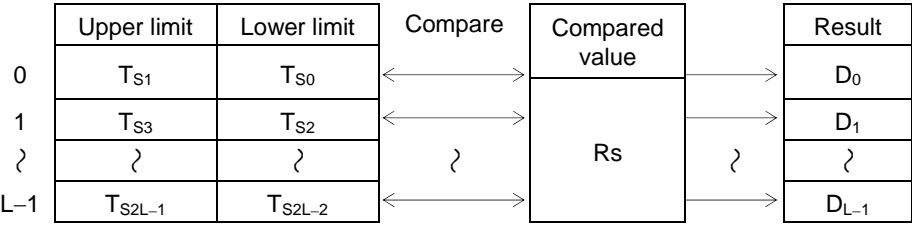
Comparison control — EN — **112DP.BKCMP** — ERR — Limit error

Rs :  Ts :  L :  D : 

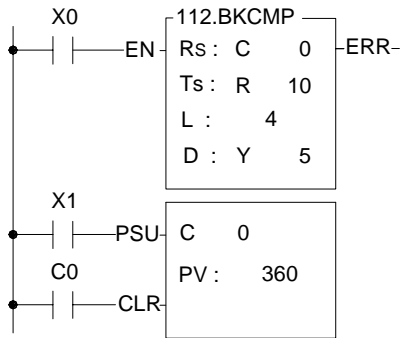
Rs : Data for compare, can be a constant or a register
Ts : Starting register block storing upper and lower limit
L : Number of pairs of upper and lower limits
D : Starting relay storing results of comparison

Range	Y	M	S	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K
Op- erand	Y0 Y255	M0 M999	S0 S999	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	16/32-bit +/- number
Rs				○	○	○	○	○	○	○	○	○	○	○	○	○
Ts				○	○	○	○	○	○	○	○	○	○	○	○	
L										○				○*	○	1~256
D	○	○	○													

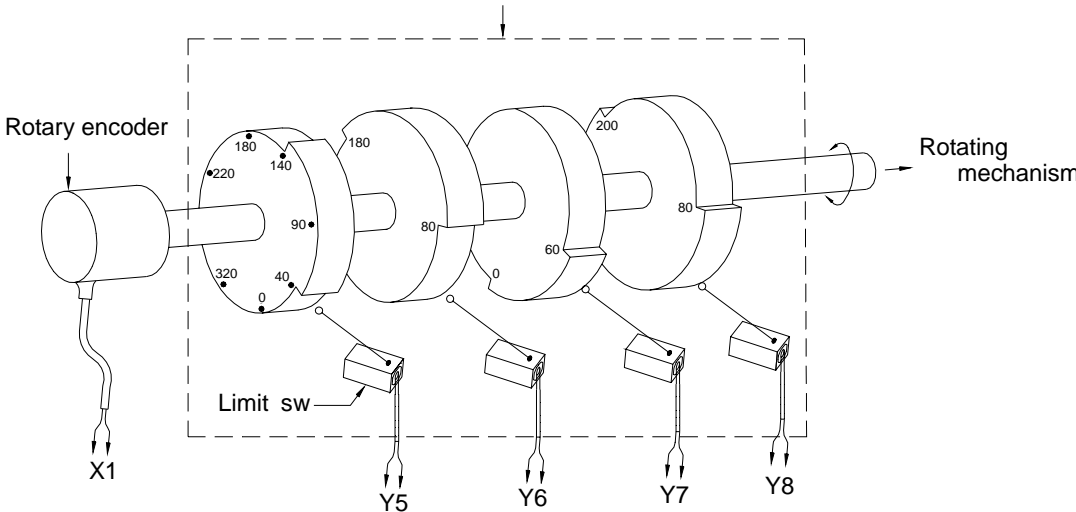
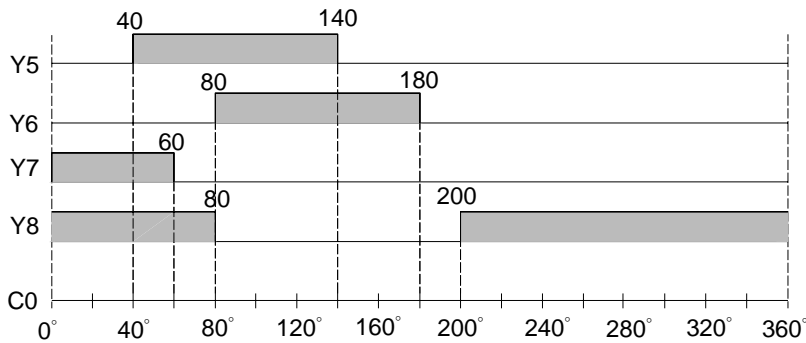
- When comparison control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), comparisons will be perform one by one between the contents of Rs and the upper and lower limits form by L pairs of 16 or 32-bit (**D** modifier) registers starting from the Ts register (starting from T0 each adjoining 2 register units form a pair of upper and lower limits). If the value of Rs falls within the range of the pair, then the bit within the comparison results relay D which corresponds to that pair will be set to 1. Otherwise it will be set as 0 until comparison of all the L pairs of upper and lower limits is completed.
- When M1975=0, if there is any pair where the upper limit value is less than the lower limit value, then the limit error flag "ERR" will be set to 1, and the comparison output for that pair will be 0.
- When M1975=1, there is no restriction on the relation of upper limit and lower limit, this can apply for 360° rotary electronic drum switch application.



- Actually this instruction is a drum switch, which can be used in interrupt program and when incorporate with immediate I/O instruction (IMDIO) can achieve an accurate electronic drum.



- In this program, C0 represents the rotation angle (Rs) of a drum shaft. The block compare instruction performs a comparison between Rs and the 4 pairs (L = 4) of upper and lower limits, R10,R11, R12,R13, R14,R15 and R16,R17. The comparison results can be obtained from the four drum output points Y5 to Y8.
- The input point X1 is a rotation angle detector mounted on the drum shaft. With each one degree rotation of the drum shaft angle, X1 produces a pulse. When the drum shaft rotates a full cycle, X1 produces 360 pulses.

FUN112 DP BKCMP	BLOCK COMPARE (DRUM)	FUN112 DP BKCMP
<ul style="list-style-type: none">● The program in the diagram above coordinates a rotary encoder or other rotating angle detection device (directly connect to a rotating mechanism), which can form a mechanical device equivalent to the mechanical structure of an actual drum (see mechanism shown within dotted line in diagram below). While the upper and lower limits are being adjusted, you can change at will the range of the activated angle of the drum. This cannot be done with the traditional drum mechanism.		
Equivalent mechanical drum emulated by above program		
		
		

FUN113 DP SORT	DATA SORTING	FUN113 DP SORT
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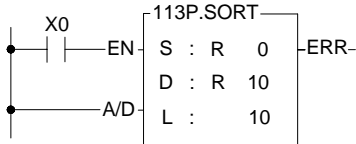
Ladder symbol



S : Starting register of source registers to sort
D : Starting register of destination registers to store the data after sorted
L : Total register for sorting

Range	TMR	CTR	HR	IR	OR	SR	ROR	DR	K
	T0	C0	R0	R3840	R3904	R3968	R5000	D0	2
	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	127
Operand									
S	○	○	○	○	○	○	○	○	
D			○				○*	○	
L			○				○	○	○

- When sort control "EN" = 1 or has a transition from 0 to 1(**P** instruction), will sort the registers with ascending order (if A/D = 1) or descending order (if A/D = 0) and put the sorted result to the registers starting by D register.
- The valid data length of sort operation is between 2 and 127, other length will set the "ERR" to 1 and the sort operation will not perform.



- The example at left sorts the table comprised of R0~R9 and stores the sorted data to the table locate at R10~R19.

S			D	
R0	1547	$X0 = \uparrow$ \Rightarrow	R10	0013
R1	2314		R11	1547
R2	7725		R12	1925
R3	0013		R13	2314
R4	5247		R14	2796
R5	1925		R15	5247
R6	6744		R16	5319
R7	5319		R17	6744
R8	9788		R18	7725
R9	2796		R19	9788
Before			After	

X0 =
 ⇒

Before

After

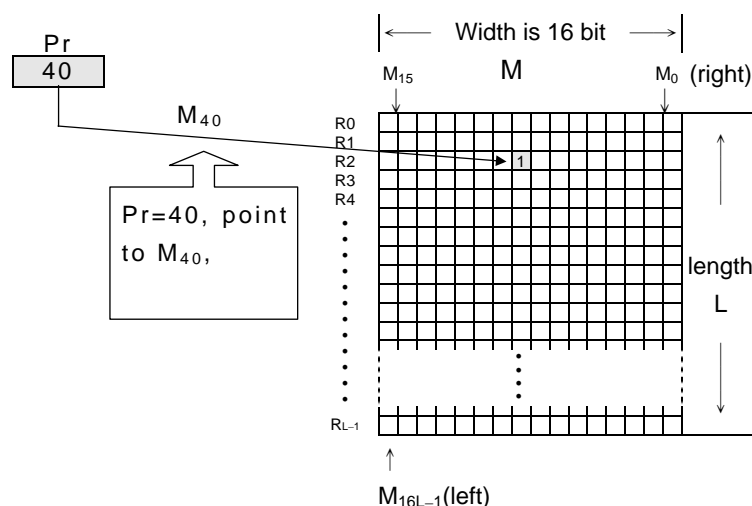
Table Instructions

FUN114 D P Z-WR		ZONE WRITE														FUN114 D P Z-WR																																																																																					
		<p><u>Ladder symbol</u></p> <div><div>Operation control — EN</div><div>Write Selection — 1/0</div></div> <div><div>114P.Z-WR</div><div>D : <div></div></div><div>N : <div></div></div></div> <div>ERR —</div>														<p>D : Starting address of being set or reset</p> <p>N : Quantity of being set or reset, 1~511</p> <p>D 、 N operand can combine V 、 Z 、 P0~P9 for index addressing while word operation</p>																																																																																					
		<table><tr><th>Range</th><th>Y</th><th>M</th><th>S</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td rowspan="2">Operand</td><td>Y0</td><td>M0</td><td>S0</td><td>WY0</td><td>WM0</td><td>WS0</td><td>T0</td><td>C0</td><td>R0</td><td>R3840</td><td>R3904</td><td>R3968</td><td>R5000</td><td>D0</td><td></td><td>V · Z</td></tr><tr><td>Y255</td><td>M1911</td><td>S99</td><td>WY240</td><td>WM1896</td><td>WS984</td><td>T255</td><td>C255</td><td>R3839</td><td>R3903</td><td>R3967</td><td>R4167</td><td>R8071</td><td>D4095</td><td></td><td>P0~P9</td></tr><tr><td>D</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td></tr><tr><td>N</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td><input type="radio"/></td><td></td><td></td><td></td><td><input type="radio"/></td><td><input type="radio"/></td><td>1-511</td><td><input type="radio"/></td></tr></table>																Range	Y	M	S	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	Operand	Y0	M0	S0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0		V · Z	Y255	M1911	S99	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9	D	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	N									<input type="radio"/>				<input type="radio"/>	<input type="radio"/>	1-511	<input type="radio"/>
Range	Y	M	S	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR																																																																																					
Operand	Y0	M0	S0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0		V · Z																																																																																					
	Y255	M1911	S99	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9																																																																																					
D	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>																																																																																					
N									<input type="radio"/>				<input type="radio"/>	<input type="radio"/>	1-511	<input type="radio"/>																																																																																					
<p>● When operation control "EN"=1 or changes from 0→1 (P instruction) , it will perform the write operation according to the input status of write selection, the specified area of registers or bits will all be reset to 0 ("1/0"=0) or set to 1("1/0"=1).</p> <div><div><div>X0</div><div>EN</div><div>— I/O</div></div><div><div>114.Z-WR</div><div>D : R0</div><div>N : 10</div></div><div>ERR—</div></div> <p>• Above example, registers R0~R9 will be reset to 0 while X0=1.</p> <div><div><div>X0</div><div>EN</div><div>— I/O</div></div><div><div>114.Z-WR</div><div>D : M5</div><div>N : 7</div></div><div>ERR—</div></div> <p>• Above example, bits M5~M11 will be reset to 0 while X0=1.</p>																																																																																																					

Matrix Instructions

Fun No.	Mnemonic	Functionality	Fun No.	Mnemonic	Functionality
120	MAND	Matrix AND	126	MBRD	Matrix Bit Read
121	MOR	Matrix OR	127	MBWR	Matrix Bit Write
122	MXOR	Matrix XOR	128	MBSHF	Matrix Bit Shift
123	MXNR	Matrix XNOR	129	MBROT	Matrix Bit Rotate
124	MINV	Matrix Inverse	130	MBCNT	Matrix Bit Count
125	MCMP	Matrix Compare			

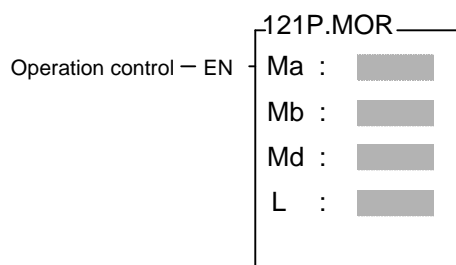
- A matrix is comprised of 2 or more consecutive 16-bit registers. The number of registers comprising the matrix is called the matrix length (L). One matrix altogether has $L \times 16$ bits (points), and the basic unit of the object for each operation is bit.
- The matrix instructions treats the $16 \times L$ matrix bits as a set of series points(denoted by M_0 to M_{16L-1}). Whether the matrix is formed by register or not, the operation object is the bit not numerical value.
- Matrix instructions are used mostly for discrete status processing such as moving, copying, comparing, searching, etc, of single point to multipoint (matrix), or multipoint-to-multipoint. These instructions are convenient, important for application.
- Among the matrix instructions, most instruction need to use a 16-bit register as a pointer to points a specific point within the matrix. This register is known as the matrix pointer (Pr). Its effective range is 0 to $16L-1$, which corresponds respectively to the bits M_0 to M_{16L-1} within the matrix.
- Among the matrix operations, there are shift left/right, rotate left/right operations. We define the movement toward higher bit is left direction, while the movement toward lower bit is right direction, as shown in the diagram below.



FUN120 P MAND	MATRIX AND	FUN120 P MAND																																																																																																								
<div><div>Ladder symbol</div><div><div>120P.MAND</div><div>Operation control —EN</div><div><div>Ma :</div><div>Mb :</div><div>Md :</div><div>L :</div></div></div></div> <div><div>Ma: Starting register of source matrix a</div><div>Mb: Starting register of source matrix b</div><div>Md : Starting register of destination matrix</div><div>L : Length of matrix (Ma, Mb and Md)</div><div>Ma, Mb, Md may combine with V, Z, P0~P9 to serve indirect address application</div></div> <table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td rowspan="2">Ope- rand</td><td>WX0</td><td>WY0</td><td>WM0</td><td>WS0</td><td>T0</td><td>C0</td><td>R0</td><td>R3840</td><td>R3904</td><td>R3968</td><td>R5000</td><td>D0</td><td>2</td><td>V · Z</td></tr><tr><td>WX240</td><td>WY240</td><td>WM1896</td><td>WS984</td><td>T255</td><td>C255</td><td>R3839</td><td>R3903</td><td>R3967</td><td>R4167</td><td>R8071</td><td>D4095</td><td>256</td><td>P0~P9</td></tr><tr><td>Ma</td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td></td><td><input type="checkbox"/></td></tr><tr><td>Mb</td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td></td><td><input type="checkbox"/></td></tr><tr><td>Md</td><td></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td></td><td><input type="checkbox"/></td><td><input checked="" type="checkbox"/></td><td><input checked="" type="checkbox"/></td><td><input type="checkbox"/></td><td></td><td><input type="checkbox"/></td></tr><tr><td>L</td><td></td><td></td><td></td><td></td><td></td><td></td><td><input type="checkbox"/></td><td></td><td></td><td></td><td><input checked="" type="checkbox"/></td><td><input type="checkbox"/></td><td><input type="checkbox"/></td><td></td></tr></table>			Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	2	V · Z	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	256	P0~P9	Ma	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		<input type="checkbox"/>	Mb	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		<input type="checkbox"/>	Md		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>		<input type="checkbox"/>	L							<input type="checkbox"/>				<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR																																																																																												
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Mb	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		<input type="checkbox"/>																																																																																												
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<div><div><div>● When operation control "EN" = 1 or has a transition from 0 to 1 (P instruction), this instruction will perform a logic AND (only if 2 bits are 1 will the result be 1, otherwise it will be 0)operation between two source matrixes with a length of L, Ma and Mb. The result will then be stored in the destination matrix Md, which is also the same length (the AND operation is done by bits with the same bit numbers). For example, if Ma₀ = 0, Mb₀ = 1, then Md₀ = 0; if Ma₁ = 1, Mb₁ = 1, then Md₁ = 1; etc, right up until AND reaches Ma_{16L-1} and Mb_{16L-1}.</div><div><div><div>Ma</div><div>Mb</div><div>Md</div><div>L</div><div>AND</div></div></div></div></div>																																																																																																										
<div><div><div><div><div>X0</div><div>EN</div></div><div>120P.MAND</div><div><div>Ma : R 0</div><div>Mb : R 10</div><div>Md : R 20</div><div>L : 5</div></div></div></div><div><div><div><div>Ma</div><div>Mb</div><div>Md</div><div>Before execution</div><div>After execution</div></div></div></div></div>																																																																																																										

FUN121 **P**
MOR

MATRIX OR

FUN121 **P**
MORLadder symbol

Ma : Starting register of source matrix a

Mb : Starting register of source matrix b

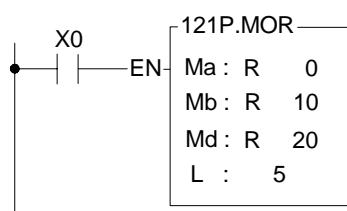
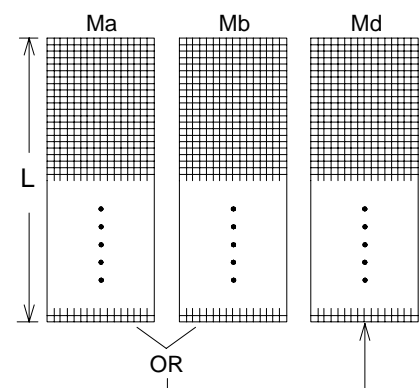
Md : Starting register of destination matrix

L : Length of matrix (Ma, Mb and Md)

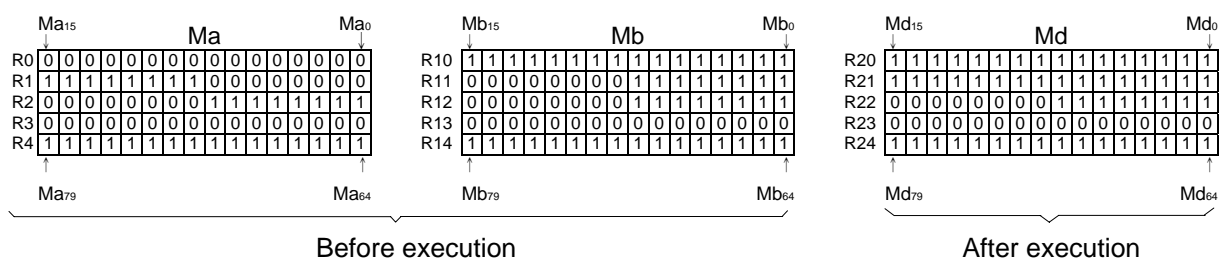
Ma, Mb, Md may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	2	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	256	P0~P9
Ma	○	○	○	○	○	○	○	○	○	○	○	○		○
Mb	○	○	○	○	○	○	○	○	○	○	○	○		○
Md		○	○	○	○	○	○		○	○*	○*	○		○
L							○				○*	○	○	

- When operation control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), this instruction will perform a logic OR (If any 2 of the bits are 1, then the result will be 1, and only if both are 0 will the result be 0) operation between 2 source matrixes with a length of L, Ma and Mb. The result will then be stored in the destination matrix Md, which is also the same length (the OR operation is done by bits with the same bit numbers). For example, if $Ma_0 = 0$, $Mb_0 = 1$, then $Md_0 = 1$; if $Ma_1 = 0$, $Mb_1 = 0$, then $Md_1 = 0$; etc, right up until OR reaches Ma_{16L-1} and Mb_{16L-1} .



- In the program at left, when X0 goes from 0→1, then matrix Ma, comprised by R0 to R4, and matrix Mb, comprised by R10 to R14, will do an OR operation. The results will then be stored into the destination matrix Md, comprised by R10 to R14. In this example, Mb and Md is the same matrix, so after operation the source matrix Mb will be replaced by the new value. The result is shown at right in the diagram below.



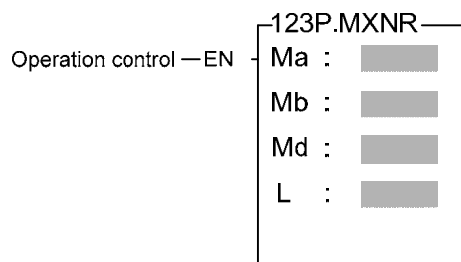
FUN122 P MXOR	MATRIX EXCLUSIVE OR (XOR)	FUN122 P MXOR																																																																																																							
<div>Ladder symbol</div> <div>Operation control—EN</div> <div>122P.MXOR</div> <div>Ma : <div></div></div> <div>Mb : <div></div></div> <div>Md : <div></div></div> <div>L : <div></div></div> <div><div>Ma: Starting register of source matrix a</div><div>Mb: Starting register of source matrix b</div><div>Md: Starting register of destination matrix</div><div>L : Length of matrix (Ma, Mb and Md)</div><div>Ma, Mb, Md may combine with V, Z, P0~P9 to serve indirect address application</div></div> <table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><th rowspan="2">Ope- rand</th><th>WX0</th><th>WY0</th><th>WM0</th><th>WS0</th><th>T0</th><th>C0</th><th>R0</th><th>R3840</th><th>R3904</th><th>R3968</th><th>R5000</th><th>D0</th><th>2</th><th>V · Z</th></tr><tr><th>WX240</th><th>WY240</th><th>WM1896</th><th>WS984</th><th>T255</th><th>C255</th><th>R3839</th><th>R3903</th><th>R3967</th><th>R4167</th><th>R8071</th><th>D4095</th><th>256</th><th>P0~P9</th></tr><tr><td>Ma</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td></tr><tr><td>Mb</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td></tr><tr><td>Md</td><td></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td><td><input checked="" type="radio"/></td><td><input checked="" type="radio"/></td><td><input type="radio"/></td><td></td><td><input type="radio"/></td></tr><tr><td>L</td><td></td><td></td><td></td><td></td><td></td><td></td><td><input type="radio"/></td><td></td><td></td><td></td><td><input checked="" type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td></td></tr></table> <div><div>● When operation control "EN" = 1 or has a transition from 0 to 1 (P instruction), this instruction will performs a logic XOR (if the 2 bits are different, then the result will be 1, otherwise it will be 0)between 2 source matrixes with a length of L, Ma and Mb. The result will then be stored back into the destination matrix Md, which also has a length of L. For example the XOR operation is done by bits with the same bit numbers - for example, if Ma₀ = 0, Mb₀ = 1, then Md₀ = 1; if Ma₁ = 1, Mb₁ = 1, then Md₁ = 0; etc, right up until XOR reaches Ma_{16L-1} and Mb_{16L-1}.</div><div><div>Ma</div><div>Mb</div><div>Md</div><div>L</div><div>XOR</div></div></div> <div><div><div>X0</div><div>●</div><div>EN</div></div><div>122P.MXOR</div><div>Ma : R 0</div><div>Mb : R 10</div><div>Md : R 20</div><div>L : 5</div></div> <div><div>● In the program at left, when X0 goes from 0→1, will perform a XOR operation between matrix Ma, comprised by R0 to R4, and matrix Mb, comprised by R10 to R14. The results will then be stored in destination matrix Md, comprised by R20 to R24. The results are shown at right in the diagram below.</div></div> <div><div><div>Ma₁₅</div><div>Ma</div><div>Ma₀</div><div>R0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>R1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>R2</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>R3</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>R4</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>Ma₇₉</div><div>Ma₆₄</div></div><div><div>Mb₁₅</div><div>Mb</div><div>Mb₀</div><div>R10</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>R11</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>R12</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>R13</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>R14</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>Mb₇₉</div><div>Mb₆₄</div></div><div><div>Md₁₅</div><div>Md</div><div>Md₀</div><div>R20</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>R21</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>1</div><div>R22</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>R23</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>R24</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>0</div><div>Md₇₉</div><div>Md₆₄</div></div><div>Before execution</div><div>After execution</div></div>		Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	2	V · Z	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	256	P0~P9	Ma	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	Mb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	Md		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input checked="" type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>		<input type="radio"/>	L							<input type="radio"/>				<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR																																																																																											
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Mb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>																																																																																											
Md		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input checked="" type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>		<input type="radio"/>																																																																																											
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FUN123 **P**
MXNR

MATRIX EXCLUSIVE NOR (XNR)

FUN123 **P**
MXNR

Ladder symbol



Ma : Starting register of source matrix a

Mb : Starting register of source matrix b

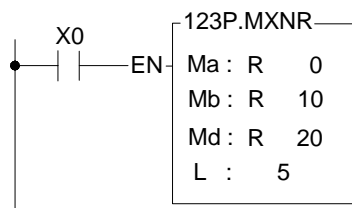
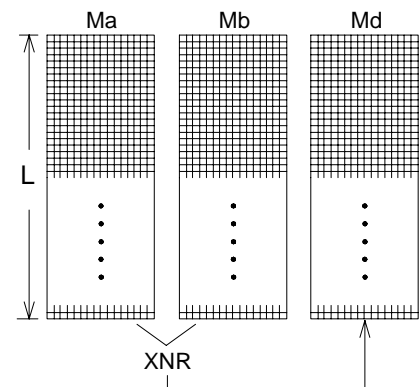
Md : Starting register of destination matrix

L : Length of matrix (Ma, Mb and Md)

Ma, Mb, Md may combine with V, Z, P0~P9 to serve indirect address application

Range Oper- and	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	2 256	V · Z P0~P9
Ma	○	○	○	○	○	○	○	○	○	○	○	○		○
Mb	○	○	○	○	○	○	○	○	○	○	○	○		○
Md		○	○	○	○	○	○		○	○*	○*	○		○
L							○				○*	○	○	

- When operation control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), will perform a logic XNR operation (if the 2 bits are the same, then the result will be 1, otherwise it will be 0) between 2 source matrixes with a length of L, Ma and Mb. The results will then be stored into the destination matrix Md, which also has the same length (the XNR operation is done by bits with the same bit numbers). For example, if $Ma_0 = 0$, $Mb_0 = 1$, then $Md_0 = 0$; $Ma_1 = 0$, $Mb_1 = 0$, then $Md_1 = 1$; etc, right up until XNR reaches Ma_{16L-1} and Mb_{16L-1} .



- When operation control "EN" = 1 or goes from 0 to 1 (**P** instruction), will perform a XNR operation between Ma matrix comprised by R0~R9 and Mb matrix comprised by R10~R19. The results will then be stored into the destination matrix Md comprised by R10~R19. The results are shown at right in the diagram below.

<div><div>Ma₁₅</div><div>Ma</div><div>Ma₀</div><div>R000</div></div>															
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FUN124 P MINV	MATRIX INVERSE	FUN124 P MINV																																																																										
<div><div>Ladder symbol</div><div>Operation control — EN</div><div>124P.MINV</div><div>Ms : <div></div></div><div>Md : <div></div></div><div>L : <div></div></div></div>		<div>Ms : Starting register of source matrix</div> <div>Md : Starting register of destination</div> <div>L : Length of matrix (Ms and Md)</div> <div>Ma, Md may combine with V, Z, P0~P9 to serve indirect address application</div>																																																																										
<table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td rowspan="2">Ope- rand</td><td>WX0 WX240</td><td>WY0 WY240</td><td>WM0 WM1896</td><td>WS0 WS984</td><td>T0 T255</td><td>C0 C255</td><td>R0 R3839</td><td>R3840 R3903</td><td>R3904 R3967</td><td>R3968 R4167</td><td>R5000 R8071</td><td>D0 D4095</td><td>2 256</td><td>V · Z P0~P9</td></tr><tr><td>Ms</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td></tr><tr><td>Md</td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td><td>○*</td><td>○*</td><td>○</td><td></td><td>○</td></tr><tr><td>L</td><td></td><td></td><td></td><td></td><td></td><td></td><td>○</td><td></td><td></td><td></td><td>○*</td><td>○</td><td>○</td><td></td></tr></table>			Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	2 256	V · Z P0~P9	Ms	○	○	○	○	○	○	○	○	○	○	○		○	Md		○	○	○	○	○	○		○	○*	○*	○		○	L							○				○*	○	○	
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR																																																														
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	Ms	○	○	○	○	○	○	○	○	○	○	○		○																																																														
Md		○	○	○	○	○	○		○	○*	○*	○		○																																																														
L							○				○*	○	○																																																															
<div><div>● When operation control "EN" = 1 or has a transition from 0 to 1 (P instruction), source register Ms, which has a length of L, will be completely inverted (all the bits with a value of 1 will change to 0, and all those with a value of 0 will change to 1). The results will then be stored into destination matrix Md.</div></div>			<div><div>Ms</div><div>Md</div><div>L</div><div>Inverse Ms</div></div>																																																																									
<div><div>X0</div><div>EN</div><div>124P.MINV</div><div>Ms : R 0</div><div>Md : R 0</div><div>L : 5</div></div>			<div><div>● In the program at left, when X0 goes from 0→1, the matrix comprised by R0 to R4 will be inverted, and then store back into itself (because in this example Ms and Md are the same matrix). The results obtained are shown at right in the diagram below.</div></div>																																																																									
<div><div>MS15</div><div>Ms</div><div>MS0</div><div>R0</div><div>R1</div><div>R2</div><div>R3</div><div>R4</div><div>MS79</div><div>MS64</div></div> <div>Before execution</div>			<div><div>Md15</div><div>Md</div><div>Md0</div><div>R0</div><div>R1</div><div>R2</div><div>R3</div><div>R4</div><div>Md79</div><div>Md64</div></div> <div>After execution</div>																																																																									

● When operation control "EN" = 1 or has a transition from 0 to 1 (P instruction), source register Ms, which has a length of L, will be completely inverted (all the bits with a value of 1 will change to 0, and all those with a value of 0 will change to 1). The results will then be stored into destination matrix Md.

Ms

L

Ms

Md

Inverse Ms

X0

EN

124P.MINV

Ms : R 0

Md : R 0

L : 5

Ms

Ms15

Ms0

Ms79

Ms64

Before execution

R0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R2	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Md

Md15

Md0

Md79

Md64

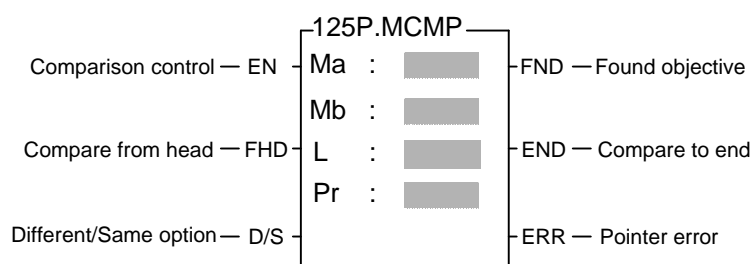
After execution

R0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R2	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

● In the program at left, when X0 goes from 0→1, the matrix comprised by R0 to R4 will be inverted, and then store back into itself (because in this example Ms and Md are the same matrix). The results obtained are shown at right in the diagram below.

FUN125 **P**
MCMP

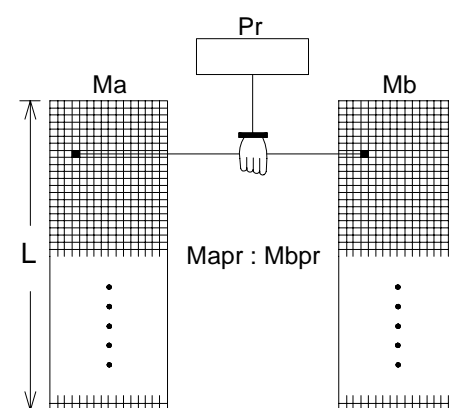
MATRIX COMPARE

FUN125 **P**
MCMPLadder symbol

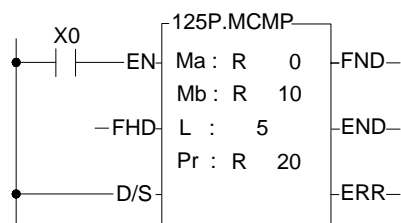
Md: Starting register of matrix a
 Mb: Starting register of matrix b
 L : Length of matrix (Ma, Mb)
 Pr : Pointer register
 Ma, Mb may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	2 256	V · Z P0~P9
Ma														
Mb														
L														
Pr														

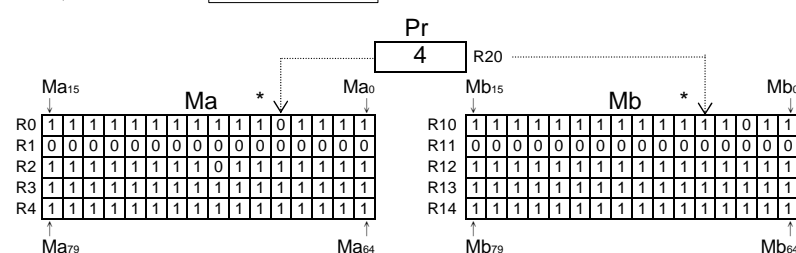
- When comparison control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), then beginning from the top pair of bits (Ma₀ and Mb₀) within the 2 matrixes Ma and Mb (when "FHD" = 1 or Pr value is equal to 16L-1), or beginning from the next pair of bits (Mapr + 1 and Mbpr + 1) pointed by pointer Pr (when "FHD" = 0 and Pr value is less than L-1), this instruction will compare and search for pairs of bits with different value (when D/S = 1) or the same value (when D/S = 0). Once match found, pointer Pr will point to the bit number in the matrix met the search condition. The found objective flag "FND" will be set to 1. When it has searched to the final pair of bits in the matrix (Ma_{16L-1}, Mb_{16L-1}), this execution of the instruction will finish, no matter it has found or not. If this happen then The compare-to-end flag "END" will be set as 1, and the Pr value will set to 16L-1 and the next time that this instruction is executed, Pr will automatically return to the starting point of the matrix (Pr = 0) to begin the comparison search.



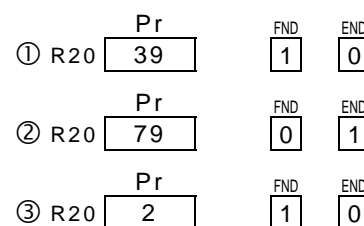
- The range for the pointer value is 0 to 16L-1. The Pr value should not be changed by other instructions, as this will affect the result of search. If the Pr value exceeds its range, then the pointer error flag "ERR" will be set to 1, and this instruction will not be carried out.



- In the program at left, the "FHD" input is 0, so starting from a position 1 greater than the pointer value at that time (marked by *), the instruction will do a search for bits with different status (because D/S = 1). When X0 has a transition from 0→1 three times, the results are shown at right in the diagram below.






Before execution



Execution result

Matrix Instructions

FUN126 P MBRD	MATRIX BIT READ	FUN126 P MBRD																																																																										
<div><div>Ladder symbol</div><div><div>126P.MBRD</div><div><div>Readout control — EN</div><div>Pointer increment — INC</div><div>Pointer clear — CLR</div></div><div><div>Ms : </div><div>L : </div><div>Pr : </div></div><div><div>OTB — Output bit</div><div>END — Read to end</div><div>ERR — Pointer error</div></div></div><div><div>Ms : Starting register of matrix</div><div>L : Matrix length</div><div>Pr : Pointer register</div><div>Ms may combine with V, Z, P0~P9 to serve indirect address application</div></div></div>																																																																												
<table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td rowspan="2">Ope- rand</td><td>WX0 WX240</td><td>WY0 WY240</td><td>WM0 WM1896</td><td>WS0 WS984</td><td>T0 T255</td><td>C0 C199</td><td>R0 R3839</td><td>R3840 R3903</td><td>R3904 R3967</td><td>R3968 R4167</td><td>R5000 R8071</td><td>D0 D4095</td><td>2 256</td><td>V · Z P0~P9</td></tr><tr><td>Ms</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td></tr><tr><td>L</td><td></td><td></td><td></td><td></td><td></td><td></td><td>○</td><td></td><td></td><td></td><td>○*</td><td>○</td><td>○</td><td></td></tr><tr><td>Pr</td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td><td>○*</td><td>○*</td><td>○</td><td></td><td></td></tr></table>			Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C199	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	2 256	V · Z P0~P9	Ms	○	○	○	○	○	○	○	○	○	○	○		○	L							○				○*	○	○		Pr		○	○	○	○	○	○		○	○*	○*	○		
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR																																																														
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	Ms	○	○	○	○	○	○	○	○	○	○	○		○																																																														
L							○				○*	○	○																																																															
Pr		○	○	○	○	○	○		○	○*	○*	○																																																																
<div><div><div>● When readout control "EN" = 1 or has a transition from 0 to 1 (P instruction), the status of the bit Mspr pointed by pointer Pr within matrix Ms will be read out and appear at the output bit "OTB". Before the readout, this instruction will first check the input -pointer clear "CLR". If "CLR" is 1, then the Pr value will be cleared to 0 first before the readout action is carried out. After the readout is completed, If the Pr value has already reached 16L-1 (the final bit), then the read-to-end flag "END" will be set to 1. If Pr is less than 16L-1, then the status of pointer increment "INC" will be checked. If "INC" is 1, then Pr will be increased by 1. Besides this, pointer clear "CLR" can execute independently, and is not affected by other input.</div><div><div>● The effective range of the pointer is 0 to 16L-1. Beyond this range the pointer error flag "ERR" will be set to 1, and this instruction will not be carried out.</div></div></div><div><div><div><div><div>X0</div><div>INC</div><div>CLR</div></div><div>126P.MBRD</div><div><div>Ms : R 0</div><div>L : 5</div><div>Pr : R 20</div></div><div><div>OTB—</div><div>END—</div><div>ERR—</div></div></div><div><div>● In the program at left, INC = 1, so every time there is one readout the pointer will be increased by 1. With this way each bit in Ms may be read out successively, as shown at left in the diagram below. When X0 goes 3 times from 0→1, the results are shown at right in the diagram below .</div></div></div><div><div><div><div><div>Ms₁₅</div><div>Ms</div><div>Ms₀</div></div><div><div>R0</div><div>R1</div><div>R2</div><div>R3</div><div>R4</div></div><div><div>0 0 0 0 0 1 1 1 1 0 0 0 0 0 1</div><div>0 0 0 0 1 1 1 1 0 0 0 0 1 1 1</div><div>0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 1</div><div>0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1</div><div>1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0</div></div><div><div>Ms₇₉</div><div>Ms₇₇</div><div>Ms₆₄</div></div></div><div><div>Pr</div><div>R20</div><div>77</div></div><div><div>OTB</div><div>0</div></div><div>Before execution</div></div><div><div><div><div>Pr</div><div>OTB</div><div>END</div></div><div><div>① R20</div><div>78</div><div>1</div><div>0</div></div><div><div>Pr</div><div>OTB</div><div>END</div></div><div><div>② R20</div><div>79</div><div>0</div><div>0</div></div><div><div>Pr</div><div>OTB</div><div>END</div></div><div><div>③ R20</div><div>79</div><div>1</div><div>1</div></div></div><div>Execution result</div></div></div></div></div>																																																																												

Pr
R20 79

OTB
1

END
1

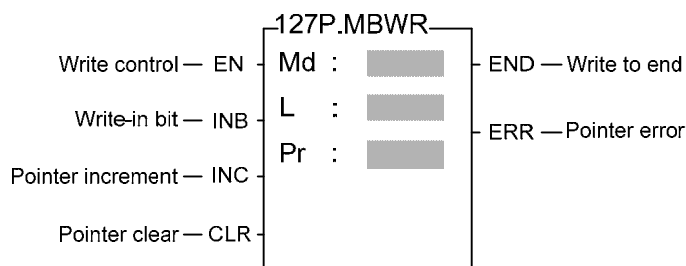
Execution result

FUN127 **P**
MBWR

MATRIX BIT WRITE

FUN127 **P**
MBWR

Ladder symbol





























Md : Starting register of matrix

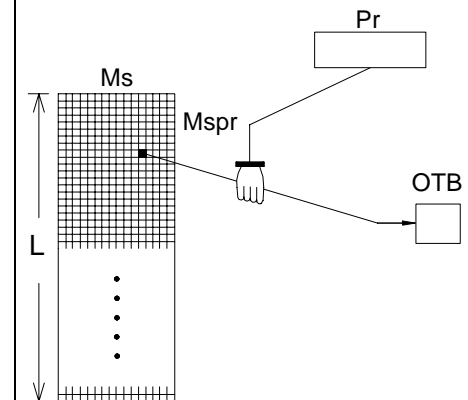
L : Matrix length

Pr : Pointer register

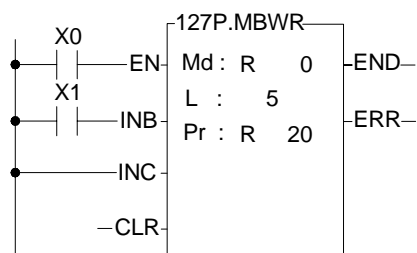
Md may combine with V, Z, P0~P9 to serve indirect address application

Range	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	K	XR
	WY0	WM0	WS0	T0	C0	R0	R3904	R3968	R5000	D0	2	V · Z
	WY240	WM1896	WS984	T255	C255	R3839	R3967	R4167	R8071	D4095	256	P0~P9
Operand												
Md												
L												
Pr												

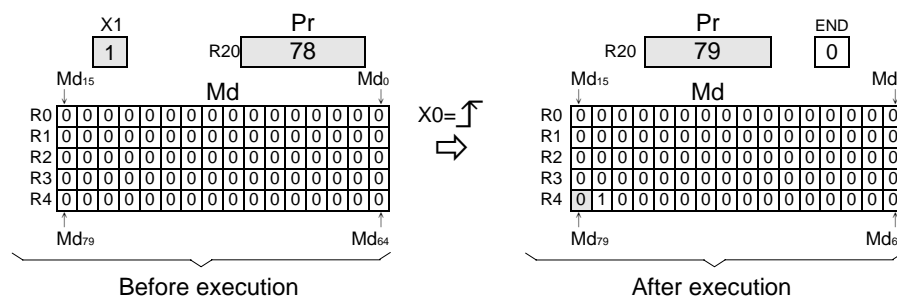
- When write control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), the status of the write-in bit "INB" will be written into the bit Md_{pr} pointed by pointer Pr within matrix Md. Before the write-in takes place, the status of pointer clear "CLR" will be checked. If "CLR" is 1, then Pr will be cleared to 0 before the write-in action. After the write-in action has been completed, the Pr value will be checked again. If the Pr value has already reached 16L-1 (last bit), then the write-to-end flag will be set to 1. If the Pr value is less than 16L-1 and "INC" is 1, then the pointer will be increased by 1. Besides this, pointer clear "CLR" can execute independently, and is not affected by other input.



- The effective range of Pr is 0 to 16L-1. Beyond this range, the pointer error flag "ERR" will be set to 1, and this instruction will not be carried out.



- In the program at left, pointer will be increased each time execution (because "INC" is 1). As shown in the diagram below, when X0 has a transition from 0→1, the status of INB (X1) will be written into the Md_{pr} (Md₇₈) position, and pointer Pr will be increased by 1 (changing to 79). In this case, although Pr is pointing to the end, it has not yet been written into Md₇₉, so "END" flag is still 0. Only the next attempt to write to Md₇₉ will set "END" to 1.



FUN128 P
MBSHF

MATRIX BIT SHIFT

FUN128 P
MBSHF

Ladder symbol

Shift control — EN

Fill-in bit — INC

Left/Right direction — CLR

128P.MBSHF

Ms :

Md :

L :

OTB — Shift out bit

Ms : Starting register of source matrix

Md: Starting register of destination matrix

L : Length of matrix (Ms and Md)

Ms, Md may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3840 R3903	R3904 R3967	R3968 R4167	R5000 R8071	D0 D4095	2 256	V · Z P0~P9
	Ms	○	○	○	○	○	○	○	○	○	○	○		○
Md		○	○	○	○	○	○		○	○*	○*	○		○
L											○*	○	○	

● When shift control "EN" = 1 or has a transition from 0 to 1 (P instruction), source matrix Ms will be retrieved and completely shifted one position to the left (when L/R = 1) or one position to the right (when L/R = 0). The space caused by the shift (with a left shift it will be M₀, and with a right shift it will be M_{16L-1}), is replaced by the status of fill-in bit "INB". The status of the bits popped out (with a left shift it will be M_{16L-1}, and with a right shift it will be M₀) will appear at the output bit "OTB". Then the results of this shifted matrix will be filled into the destination matrix Md.

● The program at left is an example where Ms and Md are the same matrix. When X0 goes from 0→1, Ms will be completely retrieved and moved to the left (because L/R = 1) by 1 bit. It will then be stored back to Md, and the results are shown at right in the diagram below.

X0

EN

X0

INB

L/R

128P.MBSHF

Ms : R 0

Md : R 0

L : 5

OTB

Ms₁₅

Ms

Ms₀

R0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

R1

1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

R2

1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0

R3

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

R4

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

MS₇₉

MS₆₄

Before execution

X0=1

⇨

Md₁₅

Md

Md₀

R0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

R1

1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

R2

1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 1

R3

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

R4

1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

Md₇₉

Md₆₄

After execution

Ms

INB

Md

Shift left 1 bit

OTB

Ms

OTB

Md

Shift right 1 bit

INB

Ms₁₅

Ms

Ms₀

R0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

R1

1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

R2

1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0

R3

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

R4

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

MS₇₉

MS₆₄

Before execution

X0=1

⇨

Md₁₅

Md

Md₀

R0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

R1

1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

R2

1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 1

R3

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

R4

1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

Md₇₉

Md₆₄

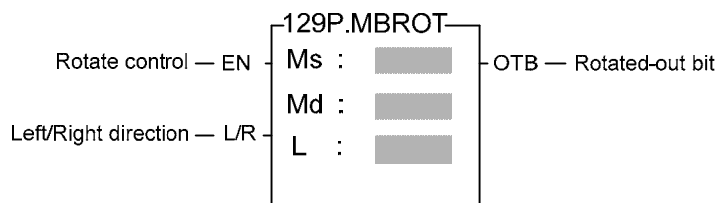
After execution

FUN129 **P**
MBROT

MATRIX BIT ROTATE

FUN129 **P**
MBROT

Ladder symbol



Ms : Starting register of source matrix

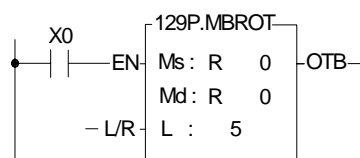
Md : Starting register of destination matrix

L : Length of matrix (Ms and Md)

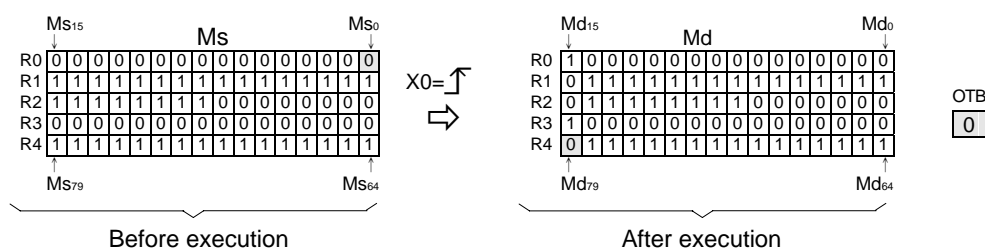
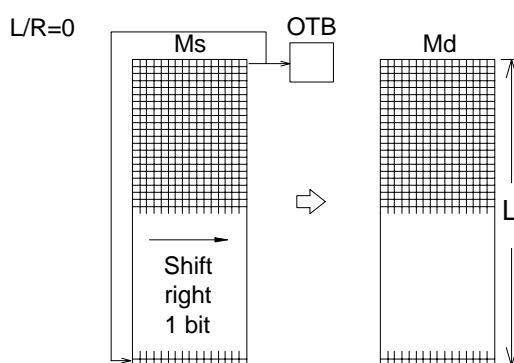
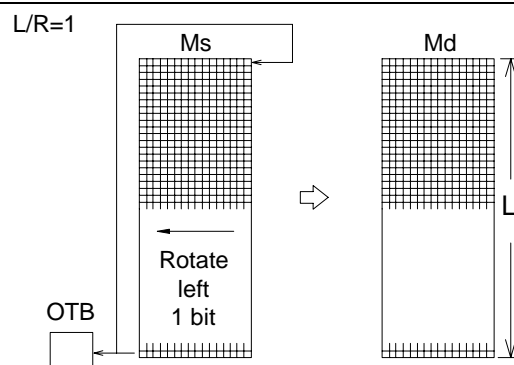
Ms, Md may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	2	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	256	P0~P9
Ms	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Md	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
L	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

- When rotate control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), matrix Ms will be completely retrieved and rotated by one bit towards the left (when L/R = 1) or to the right (when L/R = 0). The space created by the rotation (with a left rotation it will be M0, and with a right rotation it will be M_{16L-1}) will be replaced by the status of the rotated-out bit (with a left rotation it will be M_{16L-1}, and with a right rotation it will be M0). The rotated-out bit will not only be used to fill the above-mentioned space, it will also be transferred to rotated-out bit "OTB".



- In the program at left, Ms and Md are the same matrix. When X0 goes from 0→1, then the whole of Ms is retrieved and rotated right (because L/R = 0) by 1 bit. It is then stored back into Ms itself (because in this example Ms and Md are the same matrix). The results are shown at right in the diagram below.



FUN130 P
MBCNT

MATRIX BIT STATUS COUNT

FUN130 P
MBCNT

Ladder symbol

Count control — EN

1 or 0 option — 1/0

130P.MBCNT

Ms :

L :

D :

D=0 — Result is 0

Ms : Starting register of matrix

L : Matrix length

D : Register storing count results

Ms may combine with V, Z, P0~P9 to serve indirect address application

Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0	2	V · Z
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095	256	P0~P9
Ms	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>
L							<input type="radio"/>				<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	
D		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>		

●

When count control "EN" = 1 or has a transition from 0 to 1(P instruction), then among the 16L bits of the Ms matrix, this instruction will count the total amount of bits with a status of 1 (when input "1/0" = 1) or the total amount of bits with a status of 0 (when input "1/0" = 0). The results of the counting will be stored into the register specified by D. If the value of these amounts is 0, then the Result-is-0 flag "D = 0" will be set to 1.

X0

X1

EN

1/0

130P.MBCNT

Ms : R 0

L : 5

D : R 0

D=0

●

The program at left sets X1 first as 0 (to count bits with status of 0) and then as 1 (to count bits with status of 1) and let the signal X0 has a transition from 0→1 for both case, the execution results are shown at right in the diagram below .

MS15

MS0

Ms

R0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

R1

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

R2

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

R3

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

R4

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

MS79

MS64

Source matrix

①

D

64

X1=0

②

D

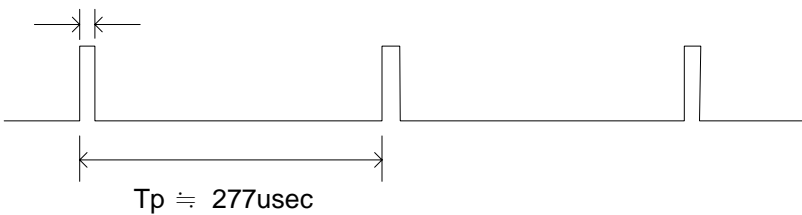
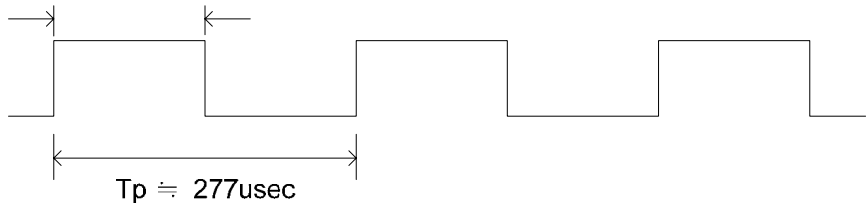
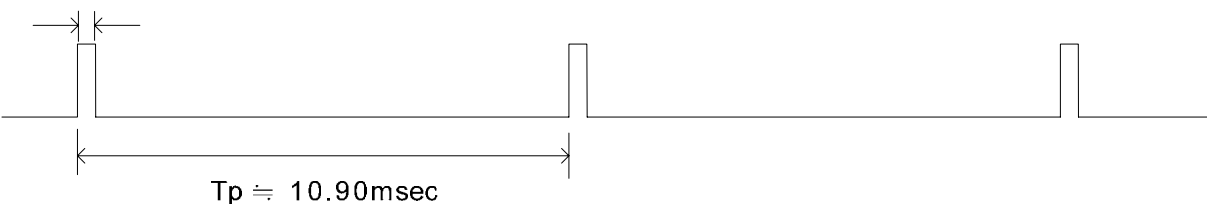

16

X1=1

Count of '0' bit

Count of '1' bit




7-127

FUN 139 HSPWM	HIGH SPEED PULSE WIDTH MODULATION OUTPUT	FUN 139 HSPWM
<p>$T_o \doteq 2.7\mu\text{sec}$</p>  <p>$T_p \doteq 277\mu\text{sec}$</p> <p>(2).Pn (Output frequency) = 50, Rs = 0 (1/100), OR (Output pulse width) = 50 :</p> <p>$T_o \doteq 140\mu\text{sec}$</p>  <p>$T_p \doteq 277\mu\text{sec}$</p> <p>Example 2 : If Pn (Setting of output frequency) = 200, Rs = 1 (1/1000), then</p> $f_{\text{pwm}} = \frac{18432}{(200 + 1)} \doteq 91.7\text{Hz}$ $T(\text{Period}) = \frac{1}{f_{\text{pwm}}} \doteq 10.9\text{mS}$ <p>For Rs = 1/1000, if OR(Setting of output pulse width) = 10, then $T_o \doteq 109\mu\text{S}$; if OR(Setting of output pulse width) = 800, then $T_o \doteq 8.72\text{mS}$</p> <p>.Output waveform :</p> <p>(1).Pn (Output frequency) = 200, Rs = 1 (1/1000), OR (Output pulse width) = 10 :</p> <p>$T_o \doteq 109\mu\text{sec}$</p>  <p>$T_p \doteq 10.90\text{msec}$</p> <p>(2).Pn (Output frequency) = 200, Rs = 1 (1/1000), OR (Output pulse width) = 800 :</p> <p>$T_o \doteq 8.72\text{msec}$</p>  <p>$T_p \doteq 10.90\text{msec}$</p>		

FUN140 HPSO	HIGH SPEED PULSE OUTPUT INSTRUCTION (Brief description on function)	FUN140 HPSO																								
<div><div><div>Ladder symbol</div><div><div>140.HPSO</div><div><div>Execution control — EN</div><div>Pause — INC</div><div>Abort — ABT</div></div><div><div>Ps : </div><div>SR : </div><div>WR : </div></div><div><div>ACT —</div><div>ERR —</div><div>DN —</div></div></div></div><div><div>Ps : The Pulse Output (0~3) selection</div><div>0:Y0 & Y1</div><div>1:Y2 & Y3</div><div>2:Y4 & Y5</div><div>3:Y6 & Y7</div><div>SR : Positioning program starting register.</div><div>WR : Starting working register of instruction operation, total 7 registers, can not used in any other part of program.</div></div><div><table><tr><th>Range</th><th>HR</th><th>DR</th><th>ROR</th><th>K</th></tr><tr><td rowspan="2">Ope- rand</td><td>R0 R3839</td><td>D0 D4095</td><td>R5000 R8071</td><td>2 256</td></tr><tr><td>Ps</td><td></td><td></td><td>0~3</td></tr><tr><td>SR</td><td></td><td></td><td></td><td></td></tr><tr><td>WR</td><td></td><td></td><td></td><td></td></tr></table></div></div>			Range	HR	DR	ROR	K	Ope- rand	R0 R3839	D0 D4095	R5000 R8071	2 256	Ps			0~3	SR					WR				
Range	HR	DR	ROR	K																						
Ope- rand	R0 R3839	D0 D4095	R5000 R8071	2 256																						
	Ps			0~3																						
SR																										
WR																										
<div>Command descriptions</div> <div><ul style="list-style-type: none">The NC positioning program of HPSO (FUN140) instruction is a program written and edited with text. The executing unit of program is divided by step (which includes output frequency, traveling distance, and transferring conditions). For one FUN140 instruction, can program 250 steps of positioning points at the most. Each step of positioning program requires 9 registers. For detailed application, please refer to Chapter 11 “The NC positioning control of FBs-PLC”.The benefits of storing the positioning program in the register is that, while in application which use the MMI (man machine interface) as the operation console can save the positioning programs to MMI. Whenever the change of the positioning programs is requested, the download of positioning program can be simply done by a series of write register commands.The NC positioning of this instruction doesn't provide the linear interpolation function.When execution control “EN”=1, if Ps0~3 is not controlled by other FUN140 instruction (the status of Ps0=M1992, Ps1=M1993, Ps2=M1994, and Ps3=M1995 is ON respectively), it will start to execute from the next step of positioning point (when goes to the last step, it will be restarted from the first step); if Ps0~3 is controlled by other FUN140 instruction (the status of Ps0=M1992, Ps1=M1993, Ps2=M1994, and Ps3=M1995 are OFF), this instruction will wait and acquires the control right of output point immediately right after other FUN140 release the output.When execution control input “EN” =0, it stops the pulse output immediately.When output pause “PAU” =1 and execution control was 1, it will pause the pulse output. When output pause “PAU” =0 and execution control is still 1, it will continue the unfinished pulse output.When output abort “ABT”=1, it will halt and stop pulse output immediately. (When the execution control input “EN” becomes 1 next time, it will restart from the first step of positioning point to execute.)While send the output pulse, the output indication “ACT” is ON.When there is an execution error, the output indication “ERR” will be ON. (The error code is stored in the error code register.)When the execution of each step of positioning program is completed, the output indication “DN” will be ON.</div> <div><div>***</div><div>The working mode of Pulse Output must be configured (without setting, Y0~Y7 will be treated as normal output) to any one of following modes, before the HPSO instruction can be worked.</div><div><div>U/D Mode: Y0 (Y2, Y4, Y6), as up pulse.</div><div>Y1 (Y3, Y5, Y7), as down pulse.</div><div>K/R Mode: Y0 (Y2, Y4, Y6), as the pulse out..</div><div>Y1 (Y3, Y5, Y7), as the direction.</div><div>A/B Mode: Y0 (Y2, Y4, Y6), as A phase pulse.</div><div>Y1 (Y3, Y5, Y7), as B phase pulse.</div></div><div><ul style="list-style-type: none">The output polarity for Pulse Output can select to be Normally ON or Normally OFF.The working mode of Pulse Output can be configured by WINPROLADDER in “Output Setup” setting page.</div></div>																										

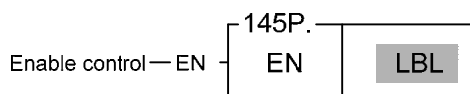
FUN141 MPARA	NC POSITIONING PARAMETER VALUE SETTING (Brief description on function)	FUN141 MPARA																								
<div><div><div><div><div><div></div><div>Ladder symbol</div></div></div><div><div><div>141.MPARA</div><div>Ps : <div></div></div><div>SR : <div></div></div></div><div><div>Execution control — EN —</div><div>— ERR —</div></div></div></div><div><div>Ps : The pulse output (0~3) selection</div><div>SR : Starting register for parameter table; it has 18 parameters totally, and occupy 24 registers.</div></div></div><div><table><tr><td>Range</td><td>HR</td><td>DR</td><td>ROR</td><td>K</td></tr><tr><td rowspan="2">Ope- rand</td><td>R0</td><td>D0</td><td>R5000</td><td>2</td></tr><tr><td>R3839</td><td>D4095</td><td>R8071</td><td>256</td></tr><tr><td>Ps</td><td></td><td></td><td></td><td>0~3</td></tr><tr><td>SR</td><td><div></div></td><td><div></div></td><td><div></div></td><td></td></tr></table></div></div>			Range	HR	DR	ROR	K	Ope- rand	R0	D0	R5000	2	R3839	D4095	R8071	256	Ps				0~3	SR	<div></div>	<div></div>	<div></div>	
Range	HR	DR	ROR	K																						
Ope- rand	R0	D0	R5000	2																						
	R3839	D4095	R8071	256																						
Ps				0~3																						
SR	<div></div>	<div></div>	<div></div>																							
<div><div>Operation descriptions</div><div><div><div>• It is not necessary to use this instruction. if the system default for parameter values is matching what user demanded, then this instruction is not needed. However, if it needs to change the parameter value dynamically, this instruction is required.</div><div>• This instruction incorporates with FUN140 or FUN147 for positioning control purpose.</div><div>• Whether the execution control input “EN” = 0 or 1, this instruction will be performed.</div><div>• When there are any errors in parameter value, the output indication “ERR” will be ON. (The error code is stored in the error code register.)</div><div>• For detailed functional description and usage, please refer to Chapter 11 “The NC positioning control of FBs-PLC” for explanation.</div></div></div></div>																										

FUN142 P PSOFF	STOP THE HPSO PULSE OUTPUT (Brief description on function)	FUN142 P PSOFF			
<div><p><u>Ladder symbol</u></p></div> <div><p>Execution control—EN</p><table border="1"><tr><td>142P.</td><td>PSOFF</td><td>Ps</td></tr></table></div> <div><p>Ps : 0~3 Enforce the Pulse Output PSON (n= Ps) to stop.</p></div>			142P.	PSOFF	Ps
142P.	PSOFF	Ps			
<div><p>Command descriptions</p></div> <div><ul style="list-style-type: none">● When execution control “EN” =1 or changes from 0→1(P instruction), this instruction will enforce the assigned number set of HPSO (High Speed Pulse Output) to stop pulse output.● While in the application for mechanical original point reset, as soon as reach the original point can use this instruction to stop the pulse output immediately, so as to make the original point stop at the same position every time when performing mechanical original point resetting.● For detailed functional description and usage, please refer to Chapter 11 “The NC positioning control of FBs-PLC” for explanation.</div>					

FUN143  PSCNV	CONVERT THE CURRENT PULSE VALUE TO DISPLAY VALUE (mm, Deg, Inch, PS) (Brief description on function)	FUN143  PSCNV																				
<div><div><div>Ladder symbol</div><div>Execution control— EN — 143P.PSCNV — Ps : <div></div> D : <div></div></div></div><div><p>Ps : 0~3; it converts the number of the pulse position to be the mm (Deg, Inch, PS) that has same unit as the set value, so as to make current position displayed.</p><p>D : Register that stores the current position after conversion. It uses 2 registers, e.g. if D = D10, which means D10 is Low Word and D11 is High Word.</p></div></div> <table><tr><th>Range</th><th>HR</th><th>DR</th><th>ROR</th><th>K</th></tr><tr><td>Ope- rand</td><td>R0 R3839</td><td>D0 D4095</td><td>R5000 R8071</td><td>2 256</td></tr><tr><td>Ps</td><td></td><td></td><td></td><td>0 ~3</td></tr><tr><td>D</td><td><div></div></td><td><div></div></td><td><div></div></td><td></td></tr></table>			Range	HR	DR	ROR	K	Ope- rand	R0 R3839	D0 D4095	R5000 R8071	2 256	Ps				0 ~3	D	<div></div>	<div></div>	<div></div>	
Range	HR	DR	ROR	K																		
Ope- rand	R0 R3839	D0 D4095	R5000 R8071	2 256																		
Ps				0 ~3																		
D	<div></div>	<div></div>	<div></div>																			
Command descriptions																						
<ul style="list-style-type: none">When execution control “En” =1 or changes from 0→1( instruction), this instruction will convert the assigned current pulse position (PS) to be the mm (or Deg, Inch, or PS) that has same unit as the set value, so as to make current position displaying.Only when the FUN140 instruction is executed, then it can get the correct conversion value by executing this instruction.For detailed functional description and usage, please refer to Chapter 11 “The NC positioning control of FBs-PLC” for explanation.																						

FUN145 **P**
EN

ENABLE CONTROL OF THE INTERRUPT AND PERIPHERAL

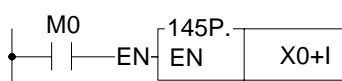
FUN145 **P**
ENLadder symbol

LBL : External input or peripheral label name that to be enabled.



- When enable control “EN” =1 or changes from 0→1 (**P** instruction), it allows the external input or peripheral interrupt action which is assigned by LBL.
- The enabled interrupt label name is as follows:(Please refer the section 9.3 for details)

LBL name	Description	LBL name	Description	LBL name	Description
HSTAI	HSTA High speed counter interrupt	X4+I	X4 positive edge interrupt	X10+I	X10 positive edge interrupt
HSC0I	HSC0 High speed counter interrupt	X4-I	X5 negative edge interrupt	X10-I	X10 negative edge interrupt
HSC1I	HSC1 High speed counter interrupt	X5+I	X5 positive edge interrupt	X11+I	X11 positive edge interrupt
HSC2I	HSC2 High speed counter interrupt	X5-I	X5 negative edge interrupt	X11-I	X11 negative edge interrupt
HSC3I	HSC3 High speed counter interrupt	X6+I	X6 positive edge interrupt	X12+I	X12 positive edge interrupt
X0+I	X0 positive edge interrupt	X6-I	X6 negative edge interrupt	X12-I	X12 negative edge interrupt
X0-I	X0 negative edge interrupt	X7+I	X7 positive edge interrupt	X13+I	X13 positive edge interrupt
X1+I	X1 positive edge interrupt	X7-I	X7 negative edge interrupt	X13-I	X13 negative edge interrupt
X1-I	X1 negative edge interrupt	X8+I	X8 positive edge interrupt	X14+I	X14 positive edge interrupt
X2+I	X2 positive edge interrupt	X8-I	X8 negative edge interrupt	X14-I	X14 negative edge interrupt
X2-I	X2 negative edge interrupt	X9+I	X9 positive edge interrupt	X15+I	X15 positive edge interrupt
X3+I	X3 positive edge interrupt	X9-I	X9 negative edge interrupt	X15-I	X15 negative edge interrupt
X3-I	X3 negative edge interrupt				

- In practical application, some interrupt signals should not be allowed to work at sometimes, however, it should be allowed to work at some other times. Employing FUN146 (DIS) and FUN145 (EN) instructions could attain the above mentioned demand.

Program example

- When M0 changes from 0→1, it allows X0 to send interrupt when X0 changes from 0→1. CPU can rapidly process the interrupt service program of X0+I.

FUN146 	DISABLE CONTROL OF THE INTERRUPT AND PERIPHERAL	FUN146 
DIS		DIS

Ladder symbol


Disable control — EN

146P.

DIS

LBL

LBL : Interrupt label intended to disable or peripheral name to be disabled.

- When prohibit control “EN” =1 or changes from 0→1 ( instruction), it disable the interrupt or peripheral operation designated by LBL.
- The interrupt label name is as follows:

LBL name	Description	LBL name	Description	LBL name	Description
HSTAI	HSTA High speed counter interrupt	X4+I	X4 positive edge interrupt	X10+I	X10 positive edge interrupt
HSC0I	HSC0 High speed counter interrupt	X4-I	X5 negative edge interrupt	X10-I	X10 negative edge interrupt
HSC1I	HSC1 High speed counter interrupt	X5+I	X5 positive edge interrupt	X11+I	X11 positive edge interrupt
HSC2I	HSC2 High speed counter interrupt	X5-I	X5 negative edge interrupt	X11-I	X11 negative edge interrupt
HSC3I	HSC3 High speed counter interrupt	X6+I	X6 positive edge interrupt	X12+I	X12 positive edge interrupt
X0+I	X0 positive edge interrupt	X6-I	X6 negative edge interrupt	X12-I	X12 negative edge interrupt
X0-I	X0 negative edge interrupt	X7+I	X7 positive edge interrupt	X13+I	X13 positive edge interrupt
X1+I	X1 positive edge interrupt	X7-I	X7 negative edge interrupt	X13-I	X13 negative edge interrupt
X1-I	X1 negative edge interrupt	X8+I	X8 positive edge interrupt	X14+I	X14 positive edge interrupt
X2+I	X2 positive edge interrupt	X8-I	X8 negative edge interrupt	X14-I	X14 negative edge interrupt
X2-I	X2 negative edge interrupt	X9+I	X9 positive edge interrupt	X15+I	X15 positive edge interrupt
X3+I	X3 positive edge interrupt	X9-I	X9 negative edge interrupt	X15-I	X15 negative edge interrupt
X3-I	X3 negative edge interrupt				

- In practical application, some interrupt signals should not be allowed to work at certain situation. To achieve this, this instruction may be used to disable the interrupt signal.

Program example

M0

146P.

DIS

X2+I

- When M0 changes from 0→1, it prohibits X2 from sending interrupt when X2 changes from 0→1.

FUN 147 MHSP0	Multi-Axis High Speed Pulse Output	FUN 147 MHSP0																								
<div><div><div><div>Ladder symbol</div><div><div><div>Execution control — EN</div><div>Pause — PAU</div><div>Abort — ABT</div></div><div><div>147.MHSP0</div><div>Gp : <div></div></div><div>SR : <div></div></div><div>WR : <div></div></div></div><div><div>ACT — Acting</div><div>ERR — Error</div><div>DN — Done</div></div></div></div><div><div>Gp : Group number (0~1)</div><div>SR : Starting register for positioning program (example explanation)</div><div>WR : Starting register for instruction operation (example explanation). It controls 9 registers, which the other program cannot repeat in using.</div></div><div><table><tr><th>Range</th><th>HR</th><th>DR</th><th>ROR</th><th>K</th></tr><tr><td rowspan="2">Ope- rand</td><td>R0 R3839</td><td>D0 D3999</td><td>R5000 R8071</td><td></td></tr><tr><td>Gp</td><td></td><td></td><td>0~1</td></tr><tr><td>SR</td><td><div></div></td><td><div></div></td><td><div></div></td><td></td></tr><tr><td>WR</td><td><div></div></td><td><div></div></td><td><div>*</div></td><td></td></tr></table></div></div></div>			Range	HR	DR	ROR	K	Ope- rand	R0 R3839	D0 D3999	R5000 R8071		Gp			0~1	SR	<div></div>	<div></div>	<div></div>		WR	<div></div>	<div></div>	<div>*</div>	
Range	HR	DR	ROR	K																						
Ope- rand	R0 R3839	D0 D3999	R5000 R8071																							
	Gp			0~1																						
SR	<div></div>	<div></div>	<div></div>																							
WR	<div></div>	<div></div>	<div>*</div>																							
<div>Instruction Explanation</div> <div><div>1. The FUN147 (MHSP0) instruction is used to support the linear interpolation for multi-axis motion control, it consists of the motion program written and edited with text programming. We named every position point as a step (which includes output frequency, traveling distance, and transfer conditions). Every step of positioning point owns 15 registers for coding.</div><div>2. The FUN147 (MHSP0) instruction can support up to 4 axes for simultaneous linear interpolation; or 2 sets of 2-axis linear interpolation (i.e. Gp0 = Axes Ps0 & Ps1 ; Gp1 = Axes Ps2 & Ps3)</div><div>3. The best benefit to store the positioning program into the registers is that in the case of association with MMI (Man Machine Interface) to operate settings, it may save and reload the positioning program via MMI when replacing the molds.</div><div>4. When execution control “EN”=1, if the other FUN147/FUN140 instructions to control Ps0~3 are not active (corresponding status of Ps0=M1992, Ps1=M1993, Ps2=M1994, and Ps3=M1995 will be ON), it will start to execute from the next step of positioning point (when goes to the last step, it will be restarted from the first step to perform); if Ps0~3 is controlled by other FUN147/FUN140 instruction (corresponding status of Ps0=M1992, Ps1=M1993, Ps2=M1994, and Ps3=M1995 would be OFF), this instruction will acquire the pulse output right of positioning control once the controlling FUN147/FUN140 has released the control right.</div><div>5. When execution control input “EN” =0, it stops the pulse output immediately.</div><div>6. When output pause “PAU” =1 and execution control “EN” was 1 beforehand, it will pause the pulse output. When output pause “PAU” =0 and execution control is still 1, it will continue the unfinished pulse output.</div><div>7. When output abort “ABT”=1, it stops pulse output immediately. (When the execution control input “EN” becomes 1 next time, it will restart from the first step of positioning point to execute.)</div><div>8. While the pulse is in output transmitting, the output indication “ACT” is ON.</div><div>9. When there is execution error, the output indication “ERR” will be ON. (The error code is stored in the error code register.)</div><div>10. When each step of positioning point is complete, the output indication “DN” will be ON.</div><div>11. Please refer to Chapter 11 “The NC Positioning Control of FBs-PLC” for further details.</div></div>																										

FUN148 MPG	MANUAL PULSE GENERATOR FOR POSITIONING		FUN148 MPG
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Execution EN —

148. MPG

Sc :

Ps :

Fo :

Mr :

WR :

— ACT

Sc : Source of high speed counter; 0~7

Ps : Axis of pulse output; 0~3

Fo : Setting of output speed (2 registers)

Mr : Setting of multiplier (2 registers)

Mr+0 : Multiplicand (Fa)

Mr+1 : Dividend (Fb)

WR : Starting address of working registers, it needs 4 registers

* This instruction can be supported in PLC OS firmware V4.60 or late

Operand \ Range	HR	ROR	DR	K
	R0	R5000	D0	16 bit
	R3839	R8071	D3999	
Sc	○	○	○	0~7
Ps	○	○	○	0~3
Fo	○	○	○	
Mr	○	○	○	
WR	○	○*	○	

- Let this instruction be executed in 50mS fixed time interrupt service routine (50MSI) · or by using the 0.1mS high speed timer to generate 50mS fixed time interrupt service to have accurate repeat time to sample the pulse input from manual pulse generator. If it comes the input pulses, it will calculate the number of pulses needing to output according to the setting of multiplier (Mr+0 and Mr+1), and then outputs the pulse stream in the speed of setting (Fo) during this time interval.

The setting of output speed (Fo) must be fast enough, and the acceleration / deceleration rate (Parameter 4 and parameter 8 of FUN141 instruction) must be sharp to guarantee it can complete the sending of pulse stream during the time interval if it is under high multiplier (100 or 200 times) situation.

- When execution “EN” =1, this instruction will sample the pulse input from manual pulse generator by reading the current value of assigned high speed counter every time interval; it doesn't have any output if it doesn't have any input pulse; but If it senses the input pulses, it will calculate the number of pulses needing to output according to the setting of multiplier (Mr+0 and Mr+1), and then outputs the pulse stream in the speed of setting (Fo) during this time interval.

Number of output pulses = (Number of input pulses × Fa) / Fb

- This instruction also under the control of hardware resource management; it wouldn't be executed if the hardware is occupied.
- The output indicator ACT=1 if it outputs the pulses; otherwise ACT=0.
- Please refer to Chapter 11 “The NC Positioning Control of FBs-PLC” for further details.

← 50mS →

- Sample pulse input
- Output pulse stream in the speed of Fo

...





← 50mS →

- Sample pulse input
- Output pulse stream in the speed of Fo

FUN150 M-BUS	MODBUS MASTER INSTRUCTION (WHICH MAKES PLC AS THE MODBUS MASTER THROUGH PORT 1~4)	FUN150 M-BUS																								
<div><div><div><div>Ladder symbol</div><div><div><div>150.M_BUS</div><div><div>Execution control — EN —</div><div>ASCII/RTU — A/R —</div><div>Abort — ABT —</div></div><div><div>Pt : <div></div></div><div>SR : <div></div></div><div>WR : <div></div></div></div><div><div>ACT —</div><div>ERR —</div><div>DN —</div></div></div></div><div><div>Pt : 1~4, specify the communication port being acted as the Modbus master</div><div>SR : Starting register of communication program</div><div>WR : Starting register for instruction operation. It controls 8 registers, the other programs can not repeat in using.</div></div><div><table><tr><th>Range</th><th>HR</th><th>ROR</th><th>DR</th><th>K</th></tr><tr><td rowspan="2">Ope- rand</td><td>R0 R3839</td><td>R5000 R8071</td><td>D0 D4095</td><td></td></tr><tr><td>Pt</td><td></td><td></td><td>1~4</td></tr><tr><td>SR</td><td><div></div></td><td><div></div></td><td><div></div></td><td></td></tr><tr><td>WR</td><td><div></div></td><td><div>*</div></td><td><div></div></td><td></td></tr></table></div></div></div></div>			Range	HR	ROR	DR	K	Ope- rand	R0 R3839	R5000 R8071	D0 D4095		Pt			1~4	SR	<div></div>	<div></div>	<div></div>		WR	<div></div>	<div>*</div>	<div></div>	
Range	HR	ROR	DR	K																						
Ope- rand	R0 R3839	R5000 R8071	D0 D4095																							
	Pt			1~4																						
SR	<div></div>	<div></div>	<div></div>																							
WR	<div></div>	<div>*</div>	<div></div>																							
<div><div>Description</div><div><div><div>1. FUN150 (M-BUS) instruction makes PLC act as Modbus master through Port 1~4, thus it is very easy to communicate with the intelligent peripheral with Modbus RTU/ASCII protocol.</div><div>2. The master PLC may connect with 247 slave stations through the RS-485 interface.</div><div>3. Only the master PLC needs to use Modbus RTU/ASCII instruction.</div><div>4. It employs the program coding method or table filling method to plan for the data flow controls; i.e. from which one of the slave station to get which type of data and save them to the master PLC, or from the master PLC to write which type of data to the assigned slave station. It needs only seven registries to make definition; every seven registers define one packet of data transaction.</div><div>5. When execution control “EN” changes from 0→1 and both inputs Pause “PAU” and Abort “ABT” are 0, and if Port 1/2/3/4 hasn’t been controlled by other communication instructions [i.e. M1960 (Port1) / M1962 (Port2) / M1936 (Port3) / M1938 (Port4) = 1], this instruction will control the Port 1/2/3/4 immediately and set the M1960/M1962/M1936/M1938 to be 0 (which means it is being occupied), then going on a packet of data transaction immediately. If Port 1/2/3/4 has been controlled (M1960/M1962/M1936/M1938 = 0), then this instruction will enter into the standby status until the controlling communication instruction completes its transaction or pause/abort its operation to release the control right (M1960/M1962/M1936/M1938 =1), and then this instruction will become enactive, set M1960/M1962/M1936/M1938 to be 0, and going on the data transaction immediately.</div><div>6. While in transaction processing, if operation control “ABT” becomes 1, this instruction will abort this transaction immediately and release the control right (M1960/M1962/M1936/M1938 = 1). Next time, when this instruction takes over the transmission right again, it will restart from the first packet of data transaction.</div><div>7. While “A/R” =0 , Modbus RTU protocol ; “A/R” =1 , Modbus ASCII protocol .</div><div>8. While it is in the data transaction, the output indication “ACT” will be ON.</div><div>9. If there is error occurred when it finishes a packet of data transaction, the output indication “DN” & “ERR” will be ON.</div><div>10. If there is no error occurred when it finishes a packet of data transaction, the output indication “DN” will be ON.</div></div></div></div>																										

FUN 151 CLINK	COMMUNICATION LINK INSTRUCTION (WHICH MAKES PLC ACT AS THE MASTER STATION IN CPU LINK NETWORK THROUGH PORT 1~4)				FUN 151 CLINK																														
<div><div><div><div>Ladder symbol</div><div><div><div>151P.CLINK</div><div><div>Execution control — EN —</div><div>Pt : <div></div></div><div>MD : <div></div></div><div>SR : <div></div></div><div>WR : <div></div></div><div>Abort — ABT —</div></div><div><div>— ACT —</div><div>— ERR —</div><div>— DN —</div></div></div></div><div><div>Pt : Assign the port, 1~4</div><div>MD : Communication mode, MD0~MD3</div><div>SR : Starting register of communication table (see example for its explanation)</div><div>WR : Starting register for instruction operation (see example for its explanation). It controls 8 registers, the other programs can not repeat in using.</div></div></div></div></div>																																			
<table><tr><td>Range</td><td>HR</td><td>ROR</td><td>DR</td><td>K</td></tr><tr><td>Ope- rand</td><td>R0 R3839</td><td>R5000 R8071</td><td>D0 D4095</td><td></td></tr><tr><td>Pt</td><td></td><td></td><td></td><td>1~4</td></tr><tr><td>MD</td><td></td><td></td><td></td><td>0~3</td></tr><tr><td>SR</td><td>○</td><td>○</td><td>○</td><td></td></tr><tr><td>WR</td><td>○</td><td>○*</td><td>○</td><td></td></tr></table>						Range	HR	ROR	DR	K	Ope- rand	R0 R3839	R5000 R8071	D0 D4095		Pt				1~4	MD				0~3	SR	○	○	○		WR	○	○*	○	
Range	HR	ROR	DR	K																															
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SR	○	○	○																																
WR	○	○*	○																																
Description																																			
<div><div><div><div><div>This instruction provides MD0~MD3. The following are the function description of respective modes.</div><div>FUN151 (CLINK) : MD 0, it makes PLC act as the master of FATEK CPU Link Network through Port 1~ 4.</div><div>The master PLC may connect with 254 slave stations through the RS485 interface.</div><div>Only the master PLC needs to use FUN151 instruction, the slave doesn't need.</div><div>It employs the program coding method or table filling method to plan for the data flow controls; i.e. from which one of the slave station to get which type of data and save them to the master PLC, or from the master PLC to write which type of data to the assigned slave station. It needs only seven registries to make definition; every seven registers define one packet of data transaction.</div><div>When execution control "EN" changes from 0→1 and both inputs "PAU" and "ABT" are 0, and if Port 1/2/3/4 hasn't been controlled by other communication instructions [i.e. M1960 (Port1) / M1962 (Port2) / M1936 (Port3) / M1938 (Port4) = 1], this instruction will control the Port 1/2/3/4 immediately and set the M1960/M1962/M1936/M1938 to be 0 (which means it is being occupied), then going on a packet of data transaction immediately. If Port 1/2/3/4 has been controlled (M1960/M1962/M1936/M1938 = 0), then this instruction will enter into the standby status until the controlling communication instruction completes its transaction or pause/abort its operation to release the control right (M1960/M1962/M1936/M1938 =1), and then this instruction will become enactive, set M1960/M1962/M1936/M1938 to be 0, and going on the data transaction immediately.</div><div>While in transaction processing, if operation control "PAU" becomes 1, this instruction will release the control right (M1960/M1962/M1936/M1938 = 1) after this transaction. Next time, when this instruction takes over the transmission right again, it will restart from the next packet of data transaction.</div><div>While in transaction processing, if operation control "ABT" becomes 1, this instruction will abort this transaction immediately and release the control right (M1960/M1962/M1936/M1938 = 1). Next time, when this instruction takes over the transmission right again, it will restart from the first packet of data transaction.</div><div>While it is in the data transaction, the output indication "ACT" will be ON.</div><div>If there is error occurred when it finishes a packet of data transaction, the output indication "DN" & "ERR" will be ON.</div><div>If there is no error occurred when it finishes a packet of data transaction, the output indication "DN" will be ON.</div><div>Please refer to Chapter 13 "The Applications for FBs-PLC Communication Link"</div></div></div></div></div>																																			

FUN160 D P RWFR		READ/WRITE FILE REGISTER																FUN160 D P RWFR																																																																																																																
<div><div><div>Ladder symbol</div><div><div>160DP.RWFR</div><div><div>Operation control — EN</div><div>Read/Write — R/W</div><div>Increment — INC</div></div><div><div>Sa : <div></div></div><div>Sb : <div></div></div><div>Pr : <div></div></div><div>L : <div></div></div></div><div>ERR — Range Error</div></div><div><div>Sa: Starting address of data register</div><div>Sb: Starting address of file register</div><div>Pr : Record pointer register</div><div>L : Quantity of register to form a record, 1~511</div><div>Sa operand can combine V、Z、P0~P9 for index addressing.</div></div></div></div>																																																																																																																																		
<table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>IR</th><th>OR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th><th>FR</th></tr><tr><td rowspan="2">Ope- rand</td><td>WX0</td><td>WY0</td><td>WM0</td><td>WS0</td><td>T0</td><td>C0</td><td>R0</td><td>R3840</td><td>R3904</td><td>R3968</td><td>R5000</td><td>D0</td><td></td><td>V、Z</td><td>F0</td></tr><tr><td>WX240</td><td>WY240</td><td>WM1896</td><td>WS984</td><td>T255</td><td>C255</td><td>R3839</td><td>R3903</td><td>R3967</td><td>R4167</td><td>R8071</td><td>D4095</td><td></td><td>P0~P9</td><td>F8191</td></tr><tr><td>Sa</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td><td></td></tr><tr><td>Sb</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>○</td></tr><tr><td>Pr</td><td></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td><td>○*</td><td>○*</td><td>○</td><td></td><td></td><td></td></tr><tr><td>L</td><td></td><td></td><td></td><td></td><td></td><td></td><td>○</td><td></td><td></td><td></td><td>○*</td><td>○</td><td>1~511</td><td></td><td></td></tr></table>																				Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	FR	Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0		V、Z	F0	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9	F8191	Sa	○	○	○	○	○	○	○	○	○	○	○	○		○		Sb															○	Pr		○	○	○	○	○	○		○	○*	○*	○				L							○				○*	○	1~511		
Range	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR	FR																																																																																																																			
Ope- rand	WX0	WY0	WM0	WS0	T0	C0	R0	R3840	R3904	R3968	R5000	D0		V、Z	F0																																																																																																																			
	WX240	WY240	WM1896	WS984	T255	C255	R3839	R3903	R3967	R4167	R8071	D4095		P0~P9	F8191																																																																																																																			
Sa	○	○	○	○	○	○	○	○	○	○	○	○		○																																																																																																																				
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Pr		○	○	○	○	○	○		○	○*	○*	○																																																																																																																						
L							○				○*	○	1~511																																																																																																																					
<div>Description</div> <div><div>●</div><div>When operation control "EN"=1 or changes from 0→1(P instruction), it will perform the read ("R/W"=1) or write ("R/W"=0) file register operation. While reading, the content of data registers starting from Sa will be overwritten by the content of file registers addressed by the base file register Sb and record pointer Pr; while writing, the content of file registers addressed by the base file register Sb and record pointer Pr will be overwritten by the content of data registers starting from Sa; L is the operation quantity or record size. The access of file register adopts the concept of RECORD data structure to implement. For example, Sa=R0, Sb=F0, L=10, the read/write details shown as below</div></div>																																																																																																																																		
<div><div><div>Sa</div><div>R0 ~ R9 (L=10)</div></div><div>↔</div><div><div>Sb</div><div><div>F0 ~ F9 (L=10)</div><div>F10 ~ F19 (L=10)</div><div>F20 ~ F29 (L=10)</div><div>F30 ~ F39 (L=10)</div><div>•</div><div>•</div><div>•</div><div>•</div><div>•</div><div>•</div></div><div><div>← Pr = 0</div><div>← Pr = 1</div><div>← Pr = 2</div><div>← Pr = 3</div></div></div></div>																																																																																																																																		

FUN160   RWFR	READ/WRITE FILE REGISTER	FUN160   RWFR
<div><ul style="list-style-type: none">● For ladder program application, only this instruction can access the file registers.● The record pointer will be increased by 1 after execution while pointer control input "INC"=1.● This instruction will not be executed and error indicator "ERR" will be 1 while incorrect record size (L=0 or > 511) or the operation out of the file register's range (F0~F8191).</div>		
<div><div><div><div><div>M0</div><div> </div><div> </div><div>EN</div></div><div><div>-R/W</div><div></div></div><div><div>INC</div><div></div></div></div><div><div>160P.RWFR</div><div>Sa : R0</div><div>Sb : F100</div><div>Pr : D0</div><div>L : 50</div></div><div><div>ERR</div><div>()</div><div>M10</div></div></div><div><p>When M0 changes from 0→1, if D0 =2, the contents of file registers F200~F249 will be overwritten by the content of data registers R0~R49. the record length is 50.</p><p>.Pointer will be increased by 1 after operation.</p></div></div>		
<div><div><div><div><div>M0</div><div> </div><div> </div><div>EN</div></div><div><div>R/W</div><div></div></div><div><div>INC</div><div></div></div></div><div><div>160P.RWFR</div><div>Sa : R0</div><div>Sb : F100</div><div>Pr : D0</div><div>L : 50</div></div><div><div>ERR</div><div>()</div><div>M10</div></div></div><div><p>.When M0 changes from 0→1, if D0 = 1, the content of data registers R0~R49 will be overwritten by the file registers F150~F199.</p><p>.The record pointer will be increased by 1 after operation.</p></div></div>		

FUN161P WR-MP	Write Data Record into the MEMORY_PACK (Write memory pack)	FUN161P WR-MP
------------------	---	------------------

Ladder symbol

Operation control — EN

Pointer Increment — INC

161P.WR-MP

S :

BK :

Os :

Pr :

L :

WR :

ACT — Acting

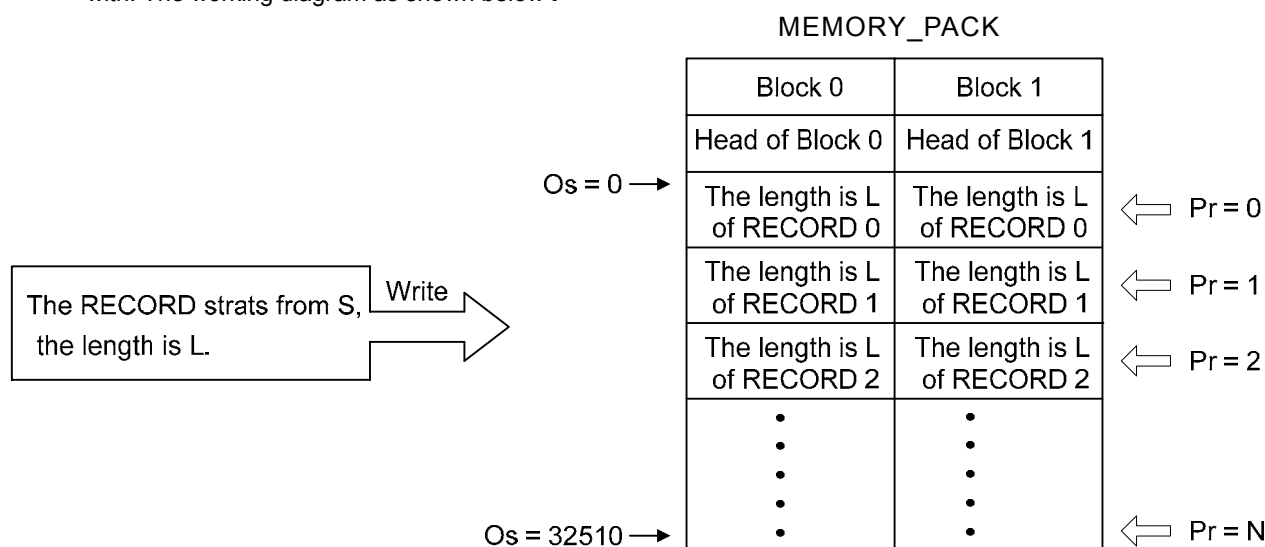
ERR — Error

DN — Done

S : Starting address of the source data
 BK : Block number of the MEMORY_PACK , 0~1
 Os : Offset of the block
 Pr : Address of the pointer
 L : Quantity of writing , 1~128
 WR : Starting address of working registers, it takes 2 registers
 S may combine with V、Z、P0~P9 for indirect addressing application

	Range	HR	ROR	DR	K	XR
Operand		R0 R3839	R5000 R8071	D0 D4095		V、Z P0~P9
S		○	○	○		○
BK					0~1	
Os		○	○	○	0~32510	
Pr		○	○*	○		
L		○	○*	○	1~128	
WR		○	○*	○		

- The main purpose of the MEMORY_PACK of FBs series's is used for long term storing of the user's ladder program, except this, through the FUN161/FUN162 instructions, the MEMORY_PACK can be worked as the portable MEMORY_PACK for machine working parameters's saving and loading.
When execution control "EN" changes from 0→1, it will perform the data writing, where S is the starting address of the source data, BK is the block number of the MEMORY_PACK to store this writing, Os is the offset of specified block, Pr is the pointer to point to corresponding data area, L is the quantity of this writing. The access of MEMORY_PACK manipulation adopts the concept of RECORD data structure to implement with. The working diagram as shown below :



- When input "INC" = 1, the content of the pointer will be increased by one after the execution of writing, it points to next record.

FUN161P
WR-MP

Write Data Record into the MEMORY_PACK
(Write memory pack)

FUN161P
WR-MP

- If the value of L is equal to 0 or greater than 128, or the pointed data area over the range, the output "ERR" will be 1, it will not perform the writing operation.
- It needs couple of PLC solving scans for data writing and verification; during the execution, the output "ACT" will be 1; when completing the execution and verification without the error, the output "DN" will be 1; when completing the execution and verification with the error, the output "ERR" will be 1.

The MEMORY_PACK can be configured to store the user's ladder program or machine's working parameters, or both. The ladder program can be stored into the block 0 only, but the machine's working parameters can be stored into block 0 or 1; the memory capacity of each block has 32K Word in total.

Example program : Writing the record into block 1 of MEMORY_PACK with the different length

M1

EN

M2

INC

161P.WR_MP

S : R0

Bk : 1

Os : 0

Pr : D1

L : 20

WR: R2900

ACT

M100

ERR

M101

DN

M102

M3

EN

M4

INC

161P.WR_MP

S : R100

Bk : 1

Os : 10000

Pr : D2

L : 50

WR: R2910

ACT

M103

ERR

M104

DN

M105

The RECORD starts from R0,
the length is 20(R0~R19)

Write

Os = 0

The RECORD starts from R100,
the length is 50(R100~R149).

Write

Os = 9999
Os = 10000

MEMORY_PACK

Block 1

Head of Block 1

The length is 20
of RECORD 0

The length is 20
of RECORD 1

⋮

The length is 20
of RECORD 499

The length is 50
of RECORD 0

⋮

The length is 50
of RECORD 449

← Pr = 0

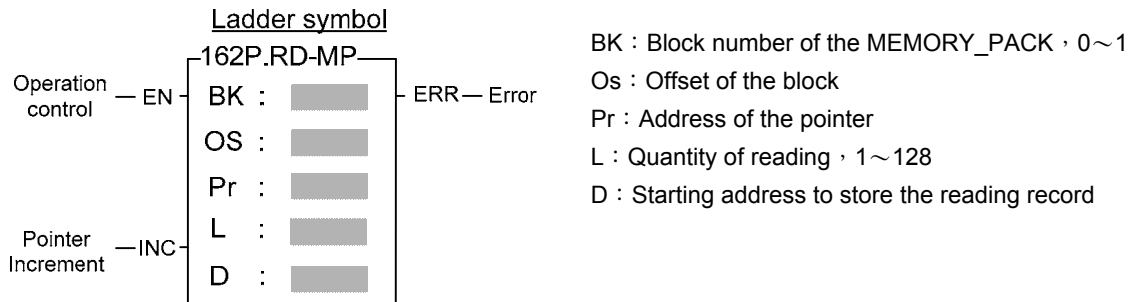
← Pr = 1

← Pr = 499

← Pr = 0

← Pr = 449

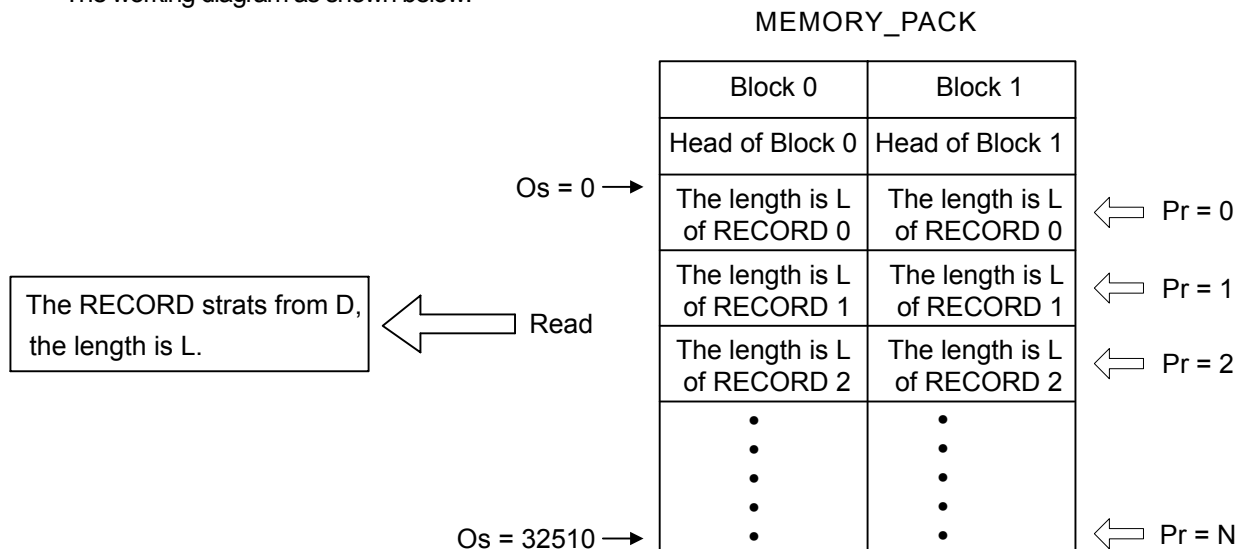
Os = 32510

FUN162 **P**
RD-MPRead Data Record from the MEMORY_PACK
(Read memory pack)FUN162 **P**
RD-MP

Operand \ Range	HR	ROR	DR	K
	R0 R3839	R5000 R8071	D0 D3999	
BK				0~1
Os	○	○	○	0~32510
Pr	○	○*	○	
L	○	○*	○	1~128
D	○	○*	○	

- If the MEMORY_PACK of the FBs series's has stored the data record written by the FUN161 instruction, they can be read out for machine's working through this instruction, it will reduce the tuning time for machine operation.
- When execution control "EN" = 1 or from 0→1(**P** instruction), it will perform the data reading, where BK is the block number of the MEMORY_PACK storing the record, Os is the offset of specified block, Pr is the pointer to point to corresponding data area, L is the quantity of this record, and D is the starting address to stor this reading of record. The access of MEMORY_PACK manipulation adopts the concept of RECORD data structure to implement with.

The working diagram as shown below:



- When input "INC"=1, the content of the pointer will be increased by one after the execution of reading, it points to next record.

FUN162 P RD-MP	Read Data Record from the MEMORY_PACK (Read memory pack)	FUN162 P RD-MP
--------------------------	---	--------------------------

- If the value of L is equal to 0 or greater than 128, or the pointed data area over the range, the output "ERR" will be 1, it will not perform the reading operation.
- Output will be "ERR" if MEMORY_PACK is empty or data format not correct, and user used FUN162 to read data from MEMORY_PACK.

Example program : Reading the record from block 1 of MEMORY_PACK with the different length

※ It is necessary that correct data in MEMORY_PACK or this example can't execute correctly.

```
graph LR
    subgraph Rung1 [ ]
        M10 -- NO --- EN1[EN]
        M11 -- NC --- INC1[INC]
        EN1 --- I1[162P.RD_MP]
        INC1 --- I1
        I1 -- Bk: 1, Os: 0, Pr: D10, L: 20, D: R0 --- ERR1[ERR]
        ERR1 --- M110((M110))
    end
    subgraph Rung2 [ ]
        M12 -- NO --- EN2[EN]
        M13 -- NC --- INC2[INC]
        EN2 --- I2[162P.RD_MP]
        INC2 --- I2
        I2 -- Bk: 1, Os: 10000, Pr: D11, L: 50, D: R100 --- ERR2[ERR]
        ERR2 --- M111((M111))
    end
```

MEMORY_PACK

Block 1	
Head of Block 1	
The length is 20 of RECORD 0	← Pr = 0
The length is 20 of RECORD 1	← Pr = 1
⋮	
The length is 20 of RECORD 499	← Pr = 499
Os = 9999 → Os = 10000 → The length is 50 of RECORD 0	← Pr = 0
⋮	
Os = 32510 → The length is 50 of RECORD 449	← Pr = 449

The RECORD starts from R0,
the length is 20(R0~R19)



Read
←

Os = 0 →

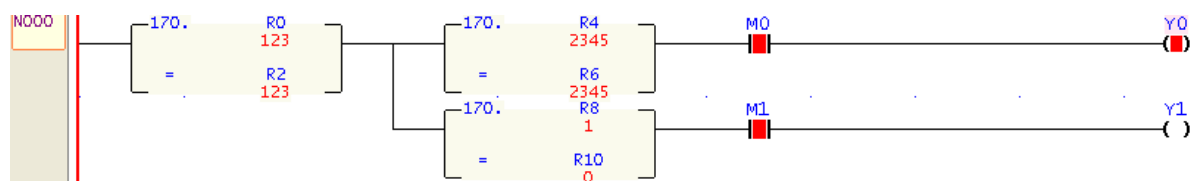
The RECORD starts from R100,
the length is 50(R100~R149)

Read
←

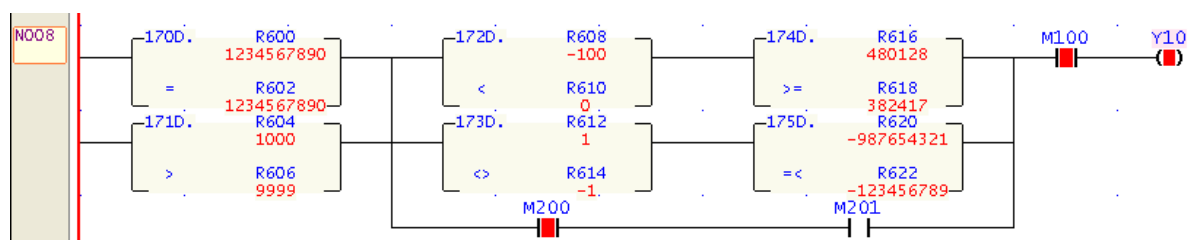
Os = 9999 →
Os = 10000 →

FUN170 	EQUAL TO COMPARE (Compare whether Sa is equal to Sb)	FUN170 																																																				
=		=																																																				
<div>Execution EN — <div><div>170D.</div><div>=</div><div>Sa Sb</div></div> —</div> <div>Sa : Operand A or the starting address of Sa Sb : Operand B or the starting address of Sb Sa 、 Sb may combine with V 、 Z 、 P0~P9 for indirect addressing application * This instruction can be supported in PLC OS firmware V4.60 or later</div>																																																						
<table><tr><th>Range Operand</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td></td><td>WX0 WX240</td><td>WY0 WY240</td><td>WM0 WM1896</td><td>WS0 WS984</td><td>T0 T255</td><td>C0 C255</td><td>R0 R3839</td><td>R3804 R4167</td><td>R5000 R8071</td><td>D0 D3999</td><td>16/ 32 bit +/- number</td><td>V 、 Z P0~P9</td></tr><tr><td>Sa</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr><tr><td>Sb</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr></table>			Range Operand	WX	WY	WM	WS	TMR	CTR	HR	SR	ROR	DR	K	XR		WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3804 R4167	R5000 R8071	D0 D3999	16/ 32 bit +/- number	V 、 Z P0~P9	Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Range Operand	WX	WY	WM	WS	TMR	CTR	HR	SR	ROR	DR	K	XR																																										
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Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																																										
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																																										

- When execution input "EN"=1, this instruction will be executed in signed number to compare Sa with Sb. If Sa=Sb, the output is 1; otherwise the output is 0.



Example 1 :

Description: When R0=R2、R4=R6 and M0=1, the output status of Y0 is 1; otherwise it is 0
R0=R2、R8=R10 and M1=1, the output status of Y1 is 1; otherwise it is 0

Example 2 :

Description: When DR600=DR602 or DR604>DR606, after them DR608<DR610 and DR616≥DR618, or DR612≠DR614 and DR620≤DR622, or M200=1 and M201=1, and then M100=1, the output status of Y10 is 1; otherwise it is 0.

In Line Comparison Instructions

FUN171 		GREATER THAN COMPARE (Compare whether Sa is greater than Sb)		FUN171 	
>				>	

Execution

EN

171D.

>

Sa
Sb

Sa : Operand A or the starting address of Sa

Sb : Operand B or the starting address of Sb

Sa 、 Sb may combine with V 、 Z 、 P0~P9 for indirect
addressing application

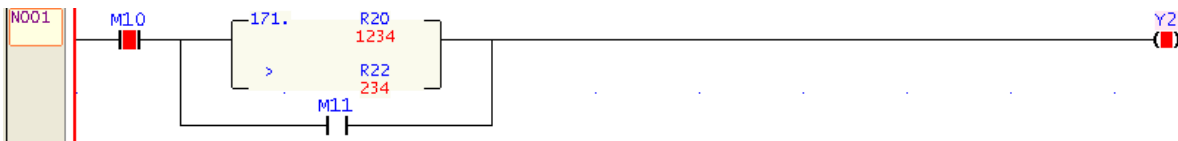
* This instruction can be supported in PLC
OS firmware V4.60 or later

Range	WX	WY	WM	WS	TMR	CTR	HR	SR	ROR	DR	K	XR
	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3804 R4167	R5000 R8071	D0 D3999	16/ 32 bit +/- number	V 、 Z P0~P9
Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

●

When execution input “EN”=1, this instruction will be executed in signed number to compare Sa with Sb. If Sa>Sb, the output is 1; otherwise the output is 0.

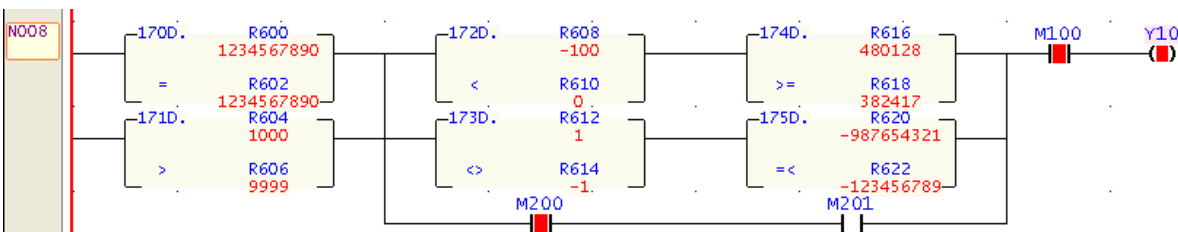
Example 1 :



Description:



When M10=1 、 R20 > R22 or M11=1, the output status of Y2 is 1; otherwise it is 0.

Example 2 :

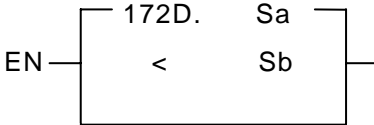


Description:

When DR600=DR602 or DR604>DR606, after them DR608<DR610 and DR616≥DR618, or DR612≠DR614 and DR620≤DR622, or M200=1and M201=1, and then M100=1, the output status of Y10 is 1; otherwise it is 0.

FUN172 	LESS THAN COMPARE (Compare whether Sa is less than Sb)	FUN172 
<		<

Execution




Sa : Operand A or the starting address of Sa
Sb : Operand B or the starting address of Sb
Sa、Sb may combine with V、Z、P0~P9 for indirect addressing application
* This instruction can be supported in PLC OS firmware V4.60 or later

Operand Range	WX	WY	WM	WS	TMR	CTR	HR	SR	ROR	DR	K	XR
	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3804 R4167	R5000 R8071	D0 D3999	16/ 32 bit +/- number	V、Z P0~P9
Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

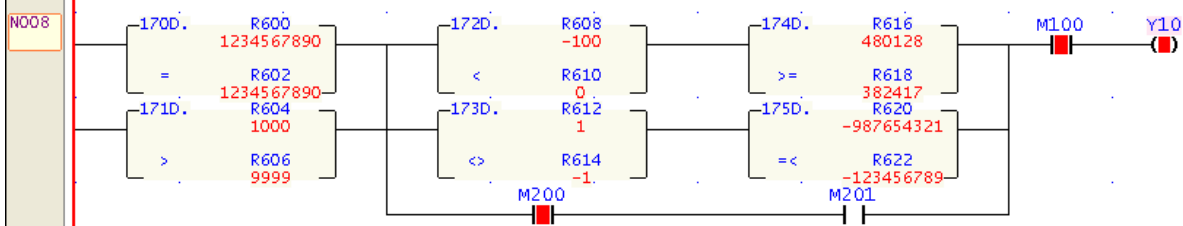
- When execution input "EN"=1, this instruction will be executed in signed number to compare Sa with Sb. If Sa<Sb, the output is 1; otherwise the output is 0.

Example 1 :





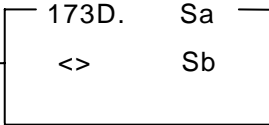
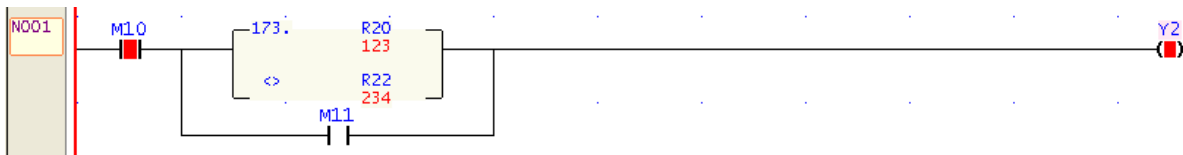
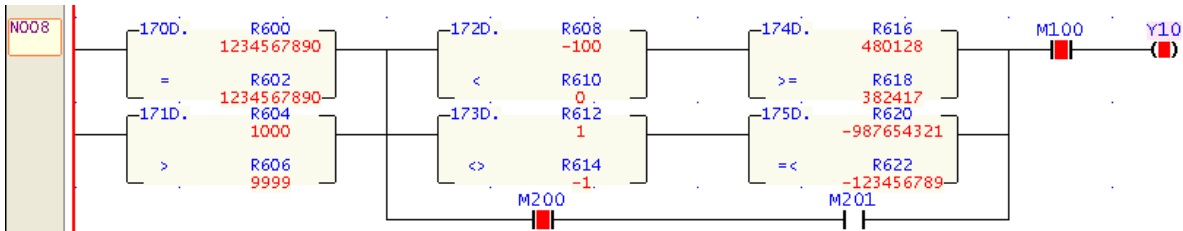
Description: When M10=1、R20 < R22 or M11=1, the output status of Y2 is 1; otherwise it is 0.



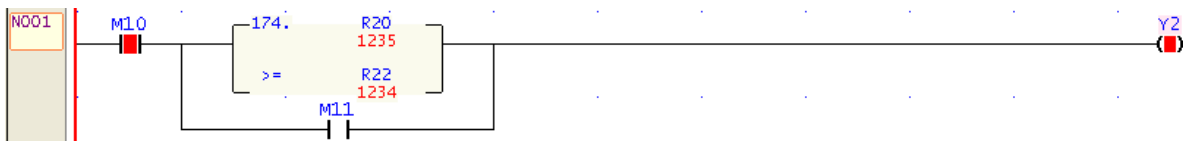
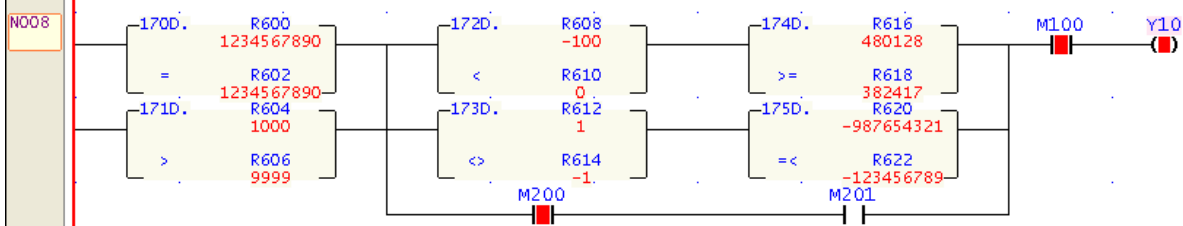
Example 2 :



Description: When DR600=DR602 or DR604>DR606, after them DR608<DR610 and DR616≥DR618, or DR612≠DR614 and DR620≤DR622, or M200=1 and M201=1, and then M100=1, the output status of Y10 is 1; otherwise it is 0.

In Line Comparison Instructions

FUN173 	NOT EQUAL TO COMPARE (Compare whether Sa is not equal to Sb)	FUN173 																																																				
<>		<>																																																				
<div>Execution EN </div> <div>Sa : Operand A or the starting address of Sa Sb : Operand B or the starting address of Sb Sa、Sb may combine with V、Z、P0~P9 for indirect addressing application * This instruction can be supported in PLC OS firmware V4.60 or later</div>																																																						
<table><tr><th>Range Operand</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td></td><td>WX0 WX240</td><td>WY0 WY240</td><td>WM0 WM1896</td><td>WS0 WS984</td><td>T0 T255</td><td>C0 C255</td><td>R0 R3839</td><td>R3804 R4167</td><td>R5000 R8071</td><td>D0 D3999</td><td>16/ 32 bit +/- number</td><td>V、Z P0~P9</td></tr><tr><td>Sa</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr><tr><td>Sb</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr></table>			Range Operand	WX	WY	WM	WS	TMR	CTR	HR	SR	ROR	DR	K	XR		WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3804 R4167	R5000 R8071	D0 D3999	16/ 32 bit +/- number	V、Z P0~P9	Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Range Operand	WX	WY	WM	WS	TMR	CTR	HR	SR	ROR	DR	K	XR																																										
	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3804 R4167	R5000 R8071	D0 D3999	16/ 32 bit +/- number	V、Z P0~P9																																										
Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																																										
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																																										
<div><div><div>●</div><div>When execution input “EN”=1, this instruction will be executed in signed number to compare Sa with Sb. If Sa≠Sb, the output is 1; otherwise the output is 0.</div></div></div>																																																						
<div><div>Example 1 :</div><div></div></div> <div>Description: When M10=1、R20≠R22 or M11=1, the output status of Y2 is 1; otherwise it is 0.</div>																																																						
<div><div>Example 2 :</div><div></div></div> <div>Description: When DR600=DR602 or DR604>DR606, after them DR608<DR610 and DR616≥DR618, or DR612≠DR614 and DR620≤DR622, or M200=1and M201=1, and then M100=1, the output status of Y10 is 1; otherwise it is 0.</div>																																																						

FUN174 	GREATER THAN OR EQUAL TO COMPARE (Compare whether Sa is greater than or equal to Sb)	FUN174 																																																			
>=		>=																																																			
<div>Execution</div> <div><div>EN</div><div><div>174D.</div><div>>=</div><div>Sa</div><div>Sb</div></div></div> <div>Sa : Operand A or the starting address of Sa Sb : Operand B or the starting address of Sb Sa 、 Sb may combine with V 、 Z 、 P0~P9 for indirect addressing application * This instruction can be supported in PLC OS firmware V4.60 or later</div> <table><tr><th>Range</th><th>WX</th><th>WY</th><th>WM</th><th>WS</th><th>TMR</th><th>CTR</th><th>HR</th><th>SR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td rowspan="2">Operand</td><td>WX0 WX240</td><td>WY0 WY240</td><td>WM0 WM1896</td><td>WS0 WS984</td><td>T0 T255</td><td>C0 C255</td><td>R0 R3839</td><td>R3804 R4167</td><td>R5000 R8071</td><td>D0 D3999</td><td>16/ 32 bit +/- number</td><td>V 、 Z P0~P9</td></tr><tr><td>Sa</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr><tr><td>Sb</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr></table>			Range	WX	WY	WM	WS	TMR	CTR	HR	SR	ROR	DR	K	XR	Operand	WX0 WX240	WY0 WY240	WM0 WM1896	WS0 WS984	T0 T255	C0 C255	R0 R3839	R3804 R4167	R5000 R8071	D0 D3999	16/ 32 bit +/- number	V 、 Z P0~P9	Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
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In Line Comparison Instructions

FUN175 D =<	LESS THAN OR EQUAL TO COMPARE (Compare whether Sa is less than or equal to Sb)	FUN175 D =<																																																				
<div> <div> Execution EN <div> <div>175D.</div> <div> Sa =< Sb </div> </div> </div> <div> Sa : Operand A or the starting address of Sa Sb : Operand B or the starting address of Sb Sa 、 Sb may combine with V 、 Z 、 P0~P9 for indirect addressing application * This instruction can be supported in PLC OS firmware V4.60 or later </div> </div>																																																						
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FUN190 STAT		READ SYSTEM STATUS				FUN190 STAT																																																																			
Execution EN		<div>190.STAT</div> <div>Gp : D :</div>		<div>Gp : Specified status group 0 : Get information of I/O expansion 1~3 : Reserved D : Starting address of register to store the system status D+0 : Quantity of status D+1 : Status 1 ... D+N: Status N</div> <div>* This instruction can be supported in PLC OS firmware V4.62 or later</div>																																																																					
<table><tr><td rowspan="2">Range Operand</td><td>HR</td><td>ROR</td><td>DR</td><td>K</td></tr><tr><td>R0 R3839</td><td>R5000 R8071</td><td>D0 D3999</td><td></td></tr><tr><td>Gp</td><td></td><td></td><td></td><td>0~3</td></tr><tr><td>D</td><td>○</td><td>○*</td><td>○</td><td></td></tr></table>		Range Operand	HR	ROR	DR	K	R0 R3839	R5000 R8071	D0 D3999		Gp				0~3	D	○	○*	○																																																						
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<div>● When execution "EN" =1, this instruction being executed, and if Gp=0, it means to get the information of I/O expansion modules; total quantity of I/O expansion modules will be stored in D register, code of I/O expansion module will be stored in D+1~D+N registers in order. Gp=1~3, reserved for future.</div>																																																																									
<table><tr><th>Code of I/O Expansion Module</th><th>Name of I/O Expansion Module</th></tr><tr><td>1</td><td>FBs-8XYR</td></tr><tr><td>2</td><td>FBs-8X</td></tr><tr><td>3</td><td>FBs-8YR</td></tr><tr><td>4</td><td>FBs-16XYR</td></tr><tr><td>5</td><td>FBs-20X</td></tr><tr><td>6</td><td>FBs-16YR</td></tr><tr><td>7</td><td>FBs-24X</td></tr><tr><td>8</td><td>FBs-24Y</td></tr><tr><td>9</td><td>FBs-24XYR</td></tr><tr><td>10</td><td>FBs-40XYR</td></tr><tr><td>11</td><td>FBs-60XYR</td></tr><tr><td>12</td><td>FBs-7SG1S (Decode)</td></tr><tr><td>13</td><td>FBs-7SG1H (Non-decode)</td></tr><tr><td>14</td><td>FBs-7SG2S (Decode)</td></tr><tr><td>15</td><td>FBs-7SG2H (Non-decode)</td></tr><tr><td>16</td><td>FBs-6AD</td></tr><tr><td>17</td><td>FBs-2DA</td></tr><tr><td>18</td><td>FBs-4DA</td></tr><tr><td>19</td><td>FBs-4PT</td></tr><tr><td>20</td><td>FBs-4A2D</td></tr></table>		Code of I/O Expansion Module	Name of I/O Expansion Module	1	FBs-8XYR	2	FBs-8X	3	FBs-8YR	4	FBs-16XYR	5	FBs-20X	6	FBs-16YR	7	FBs-24X	8	FBs-24Y	9	FBs-24XYR	10	FBs-40XYR	11	FBs-60XYR	12	FBs-7SG1S (Decode)	13	FBs-7SG1H (Non-decode)	14	FBs-7SG2S (Decode)	15	FBs-7SG2H (Non-decode)	16	FBs-6AD	17	FBs-2DA	18	FBs-4DA	19	FBs-4PT	20	FBs-4A2D	<table><tr><th>Code of I/O Expansion Module</th><th>Name of I/O Expansion Module</th></tr><tr><td>21</td><td>FBs-6TC</td></tr><tr><td>22</td><td>FBs-6RTD</td></tr><tr><td>23</td><td>FBs-16TC</td></tr><tr><td>24</td><td>FBs-16RTD</td></tr><tr><td>25</td><td>FBs-2TC</td></tr><tr><td>26</td><td>FBs-2A4TC</td></tr><tr><td>27</td><td>FBs-2A4RTD</td></tr><tr><td>28</td><td>FBs-6NTC</td></tr><tr><td>29</td><td>FBs-16NTC (Reserved)</td></tr><tr><td>30</td><td>FBs-32DGI</td></tr><tr><td>31</td><td>FBs-VOM</td></tr><tr><td>32</td><td>FBs-1LC</td></tr></table>				Code of I/O Expansion Module	Name of I/O Expansion Module	21	FBs-6TC	22	FBs-6RTD	23	FBs-16TC	24	FBs-16RTD	25	FBs-2TC	26	FBs-2A4TC	27	FBs-2A4RTD	28	FBs-6NTC	29	FBs-16NTC (Reserved)	30	FBs-32DGI	31	FBs-VOM	32	FBs-1LC
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FUN190 STAT	READ SYSTEM STATUS	FUN190 STAT																														
Example : There are two I/O expansion modules FBs-2DA + FBs-6AD installed in one system																																
<div><div><div>N003</div><div>M500</div></div><div>EN</div><div><div>190.STAT</div><div>Gp: 0</div><div>0</div><div>D : D200</div><div>2</div></div></div>																																
<div><div>Status Monitoring</div><table><tr><th>Ref. No.</th><th>Status</th><th>Data</th><th>Ref. No.</th><th>Status</th><th>Data</th></tr><tr><td>M500</td><td>Enable</td><td>ON</td><td></td><td></td><td></td></tr><tr><td>D200</td><td>Decimal</td><td>2</td><td></td><td></td><td></td></tr><tr><td>D201</td><td>Decimal</td><td>17</td><td></td><td></td><td></td></tr><tr><td>D202</td><td>Decimal</td><td>16</td><td></td><td></td><td></td></tr></table></div>			Ref. No.	Status	Data	Ref. No.	Status	Data	M500	Enable	ON				D200	Decimal	2				D201	Decimal	17				D202	Decimal	16			
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D202	Decimal	16																														
<div>Description: When M500=1, this instruction being executed, register D200 is used to store the total quantity of I/O expansion modules, register D201 is used to store the code (17=FBs-2DA) of first I/O expansion module, register D202 is used to store the code (16=FBs-6AD) of second I/O expansion module.</div>																																

FUN200 **D** **P**
I→F

CONVERSION OF INTEGER TO FLOATING POINT NUMBER

FUN200 **D** **P**
I→F

Ladder symbol

Conversion control — EN

200DP.I→F

S :

D :

S : Starting register of Integer to be converted

D : Starting register to store the result of conversion

Range	HR	ROR	DR	K	XR
	R0	R5000	D0	16/32 bit Integer	V、Z
Operand	R3839	R8071	D4095	Integer	P0~P9
S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
D	<input type="radio"/>	<input type="radio"/> *	<input type="radio"/>		<input type="radio"/>

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System)...page 5-9.
- When conversion control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), will convert the integer data from S register into D~D+1 32-bits register(floating point number data)

X0

•

—|

—|

—EN

200P.I→F

S : R0

D : D0

※ R0 = 200 (0000000011001000)

Integer To Floating ←

→ DD0 = 43480000H

R0 :

0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

I→F

DD0 :

0	1	0	0	0	0	1	1	0	1	0	0	1	0	0	0	00...0	0	
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16	b15	b14~b1	b0
s	e	e	e	e	e	e	e	e	m	m	m	m	m	m	m	m	mm...m	m

Floating Point Instructions

FUN201
F→I

201DP.F→I

Conversion control — EN

S :

D :

ERR — Range Error

FUN201
F→I

CONVERSION OF FLOATING POINT NUMBER TO INTEGER

Ladder symbol

S : Starting register of Integer to be converted

D : Starting register to store the result of conversion

Range	HR	ROR	DR	XR
	R0	R5000	D0	V · Z
Operand	R3839	R8071	D4095	P0~P9
S	<div></div>	<div></div>	<div></div>	<div></div>
D	<div></div>	<div>*</div>	<div></div>	<div></div>

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System)...page 5-9.
- When conversion control "EN" = 1 or has a transition from 0 to 1 (**P** instruction), will convert the floating point data from S~S+1 32bits register into D register(integer data).
- If the value exceeds the valid range of destination, then do not carry out this instruction, and set the range-error flag "ERR" as 1 and the D register will be intact.

X2

201P.F→I

EN

S : R20

D : D10

ERR

※ DR20 = 123.45 →Normalize→ 42F6E666H

Floating To Integer ←

→ D10 = 007BH

DR20:

0	1	0	0	0	0	1	0	1	1	1	1	0	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
s	e	e	e	e	e	e	e	e	m	m	m	m	m	m	m	m	m	m	m	m	m	m	m	m	m	m	m	m	m	m	

F → I

D10:

0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

FUN202 P FADD	FLOATING POINT NUMBER ADDITION		FUN202 P FADD																														
<p><u>Ladder symbol</u></p> <div style="display: flex; align-items: center;"> <div style="margin-right: 10px;">Addition control — EN</div> <div style="border: 1px solid black; padding: 5px; margin-right: 10px;"> 202P.FADD Sa : Sb : D : </div> <div style="margin-left: 10px;">ERR — Ranger Error (FO0)</div> </div>																																	
<p>Sa: Augend Sb: Addend D : Destination register to store the results of the addition Sa, Sb, D may combine with V, Z, P0~P9 to serve indirect addressing</p>																																	
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Sb	○	○	○	○	○																												
D	○	○*	○		○																												
<p>Description</p> <ul style="list-style-type: none"> The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System)...page 5-9. Performs the addition of the data specified at Sa and Sb and writes the results to a specified register D when the add control input "EN" =1 or from 0 to 1 (P instruction). If the result exceed the range that the floating point number can be expressed($\pm 3.4 \times 10^{38}$) then the error flag FO0 will be set to 1 and the D register will be intact. <div style="margin-top: 20px;"> </div> <div style="margin-top: 20px;"> <div style="display: flex; align-items: center; margin-bottom: 10px;"> <div style="border: 1px solid black; padding: 5px; margin-right: 10px;">DR0 2 0 0</div> <div style="font-size: 24px; margin: 0 10px;">⇒</div> <div style="margin-right: 10px;">Floating Point Number :</div> <div style="border: 1px solid black; padding: 5px; margin-left: 10px;">DR0 4 3 4 8 0 0 0 0 H</div> </div> <div style="display: flex; align-items: center; margin-bottom: 10px;"> <div style="border: 1px solid black; padding: 5px; margin-right: 10px;">DR10 1 5 0</div> <div style="font-size: 24px; margin: 0 10px;">⇒</div> <div style="margin-right: 10px;">Floating Point Number :</div> <div style="border: 1px solid black; padding: 5px; margin-left: 10px;">DR10 4 3 1 6 0 0 0 0 H</div> </div> <div style="text-align: center; margin-bottom: 10px;"> <div style="font-size: 24px; margin: 0 10px;">+</div> <hr style="width: 100%; border: 0.5px solid black;"/> </div> <div style="display: flex; align-items: center;"> <div style="border: 1px solid black; padding: 5px; margin-right: 10px;">DR20</div> <div style="border: 1px solid black; padding: 5px;">4 3 A F 0 0 0 0 H</div> </div> </div>																																	

FUN 203 P
FSUB

FLOATING POINT NUMBER SUBTRACTION

FUN 203 P
FSUB

Ladder symbol

Subtraction control — EN

203P.FSUB

Sa :

Sb :

D :

ERR — Ranger Error (FO0)

Sa: Minuend

Sb: Subtrahend

D : Destination register to store the results
of the subtraction

Sa, Sb, D may combine with V, Z, P0~P9 to
serve indirect addressing

Range	HR	ROR	DR	K	XR
	R0 R3839	R5000 R8071	D0 D4095	Floating point number	V、Z P0~P9
Operand					
Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
D	<input type="radio"/>	<input type="radio"/> *	<input type="radio"/>		<input type="radio"/>

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System)...page 5-9.
- Performs the subtraction of the data specified at Sa and Sb and writes the results to a specified register D when the subtract control input "EN" =1 or from 0 to 1 (P instruction). If the result exceed the range that the floating point number can be expressed($\pm 3.4 \times 10^{38}$) then the error flag FO0 will be set to 1 and the D register will be intact.

X0

EN

203P.FSUB

Sa : R0

Sb : R4

D : R10

ERR

DR0

2 0 0

⇒ Floating Point Number :

DR0

4 3 4 8 0 0 0 0 H

DR4

5 0 0

⇒ Floating Point Number :

DR4

4 3 F A 0 0 0 0 H

DR10

C 3 9 6 0 0 0 0 H

7-157

FUN 204 P FMUL

FLOATING POINT NUMBER MULTIPLICATION

FUN 204 P FMUL

Ladder symbol

Multiplication control — EN

204P.FMUL

Sa :

Sb :

D :

ERR — Ranger Error (FO0)

Sa: Multiplicand

Sb: Multiplier

D : Destination register to store the results of the multiplication

Sa, Sb, D may combine with V, Z, P0~P9 to serve indirect addressing

Range	HR	ROR	DR	K	XR
	R0 R3839	R5000 R8071	D0 D4095	Floating point number	V、Z P0~P9
Operand					
Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
D	<input type="radio"/>	<input type="radio"/> *	<input type="radio"/>		<input type="radio"/>

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System)...page 5-9.
- Performs the multiplication of the data specified at Sa and Sb and writes the results to a specified register D when the multiplication control input "EN" =1 or from 0 to 1 (P instruction). If the result exceed the range that the floating point number can be expressed($\pm 3.4 \times 10^{38}$) then the error flag FO0 will be set to 1 and the D register will be intact.

M10

—| |— EN

204P.FMUL

Sa : R10

Sb : R12

D : R14

ERR—

DR10

1 2 3 . 4 5

⇒ Floating Point Number :

DR10

4 2 F 6 E 6 6 6 H

DR12

6 7 8 . 5 4

⇒ Floating Point Number :

DR12

4 4 2 9 A 2 8 F H

×

DR14

4 7 A 3 9 A E 2 H

FUN 205 P
FDIV

FLOATING POINT NUMBER DIVISION

FUN 205 P
FDIV

Ladder symbol

Division control — EN

205P.FDIV

Sa :

Sb :

D :

ERR — Ranger Error (FO0)

Sa: Dividend

Sb: Divisor

D : Destination register to store the results of the division

Sa, Sb, D may combine with V, Z, P0~P9 to serve indirect addressing

Range	HR	ROR	DR	K	XR
	R0 R3839	R5000 R8071	D0 D4095	Floating point number	V、Z P0~P9
Operand					
Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
D	<input type="radio"/>	<input type="radio"/> *	<input type="radio"/>		<input type="radio"/>

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System) page 5-9.
- Performs the division of the data specified at Sa and Sb and writes the result to the registers specified by register D when the division control input "EN" =1 or from 0 to 1 (**P** instruction). If the result exceed the range that the floating point number can be expressed($\pm 3.4 \times 10^{38}$) then the error flag FO0 will be set to 1 and the D register will be intact.

X5

EN

205P.FDIV

Sa : R0

Sb : R2

D : R4

ERR—

DR0

1 2 5 . 2 5

⇒ Floating Point Number :

DR0

4 2 F A 8 0 0 0 H

DR2

5

⇒ Floating Point Number :

DR2

4 0 A 0 0 0 0 0 H

÷

DR4

4 1 C 8 6 6 6 6 H

FUN 206 **P**
FCMP

FLOATING POINT NUMBER COMPARE

FUN 206 **P**
FCMP

Ladder symbol

Compare control — EN

206P.FCMP

Sa :

Sb :

a = b — Sa=Sb (FO0)

a > b — Sa>Sb (FO1)

a < b — Sa<Sb (FO2)

Sa: The register to be compared

Sb: The register to be compared

Sa, Sb may combine with V, Z, P0~P9 to serve indirect addressing.

Range	HR	ROR	DR	K	XR
	R0 R3839	R5000 R8071	D0 D4095	Floating point number	V、Z P0~P9
Operand					
Sa	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
Sb	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System) page 5-9.
- Compares the data of Sa and Sb when the compare control input "EN" =1 or from 0 to 1 (**P** instruction). If the data of Sa is equal to Sb, then set FO0 to 1. If the data of Sa>Sb, then set FO1 to 1. If the data of Sa<Sb, then set FO2 to 1. If the data of Sa < Sb, then set the FO2 to 1.

X0

—|

—|

—EN

206P.FCMP

Sa : R0

Sb : R2

a=b —

a>b — Y0

a<b — ()

DR0

200.1

⇒ Floating Point Number :

DR0

4348199AH

DR2

200.2

⇒ Floating Point Number :

DR2

43483333H

- From the above example, we first assume the data of DR0 is 200.1 and DR2 is 200.2, and then compare the data by executing the CMP instruction. The FO0 and FO1 are set to 0 and FO2 (a<b) is set to 1 since a<b.
- If you want to have the compound results, such as ≥、≤、< > etc., please send =< and > results to relay first and then combine the result from the relays.

FUN 207 P FZCP		FLOATING POINT NUMBER ZONE COMPARE		FUN 207 P FZCP																																					
<div><div>Ladder Symbol</div><div><div>Compare control — EN</div><div>207P.FZCP</div><div>S : <div></div> — INZ — Inside zone</div><div>Su : <div></div> — S>U — Higher than upper limit</div><div>SL : <div></div> — S<L — Lower than lower limit</div><div>ERR — Limit value erroe</div></div></div> <div><div>S : Register for zone comparison</div><div>Su: The upper limit value</div><div>SL: The lower limit value</div><div>S, Su, SL may combine with V, Z, P0~P9 to serve indirect address application</div></div> <div><table><tr><th>Range</th><th>HR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td></td><td>R0 R3839</td><td>R5000 R8071</td><td>D0 D4095</td><td>Floating point number</td><td>V、Z P0~P9</td></tr><tr><th>Operand</th><td></td><td></td><td></td><td></td><td></td></tr><tr><td>S</td><td><div></div></td><td><div></div></td><td><div></div></td><td><div></div></td><td><div></div></td></tr><tr><td>Su</td><td><div></div></td><td><div></div></td><td><div></div></td><td><div></div></td><td><div></div></td></tr><tr><td>SL</td><td><div></div></td><td><div></div></td><td><div></div></td><td><div></div></td><td><div></div></td></tr></table></div>						Range	HR	ROR	DR	K	XR		R0 R3839	R5000 R8071	D0 D4095	Floating point number	V、Z P0~P9	Operand						S	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>	Su	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>	SL	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>
Range	HR	ROR	DR	K	XR																																				
	R0 R3839	R5000 R8071	D0 D4095	Floating point number	V、Z P0~P9																																				
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Su	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>																																				
SL	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>																																				
<div>Description</div> <div><ul style="list-style-type: none">The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System) page 5-9.When compare control "EN" = 1 or changes from 0 to 1 (P instruction), compares S with upper limit SU and lower limit SL. If S is between the upper limit and the lower limit ($S_L \leq S \leq S_U$), then set the inside zone flag "INZ" to 1. If the value of S is greater than the upper limit S_U, then set the higher than upper limit flag "S>U" to 1. If the value of S is smaller then the lower limit S_L, then set the lower than lower limit flag "S<L" as 1.The upper limit S_U should be greater than the lower limit S_L. If $S_U < S_L$, then the limit value error flag "ERR" will set to 1, and this instruction will not carry out.</div> <div><div><div>X0</div><div><div></div><div>EN</div></div><div>207P.FZCP</div><div><div>S : R10</div><div>Su : R12</div><div>SL : R14</div></div><div><div>INZ — ()</div><div>S>U —</div><div>S<L —</div><div>ERR —</div></div><div>Y0</div></div><div><ul style="list-style-type: none">The instruction at left compares the value of DR10 with the upper and lower limit zones formed by DR12 and DR14. If the values of DR10~DR14 are as shown in the diagram at bottom left, then the result can then be obtained as at the right of this diagram.If want to get the status of out side the zone, then OUT NOT Y0 may be used, or an OR operation between the two outputs S>U and S<L may be carried out, and move the result to Y0.</div></div>																																									

FUN 207 P FZCP	FLOATING POINT NUMBER ZONE COMPARE	FUN 207 P FZCP
--------------------------	------------------------------------	--------------------------

S	DR10	2 0 0 0 . 2
Su	DR12	3 0 0 0 . 3
SL	DR14	1 0 0 0 . 1

⇒ Floating Point Number :

DR10	4 4 F A 0 6 6 6 H
DR12	4 5 3 B 8 4 C D H
DR14	4 4 7 A 0 6 6 6 H

(Upper limit value)
(Lower limit value)

Before-execution

X0 = → FLOATING ZONE COMPARE → Y0 = 1

Results of execution

FUN 208 P FSQR	FLOATING POINT NUMBER SQUARE ROOT	FUN 208 P FSQR																																			
<div><div><div>Ladder symbol</div><div>208P.FSQR</div><div>Operation control — EN — S : <div></div> — ERR — S range error</div><div>D : <div></div></div></div><div><div>S : Source register to be taken square root</div><div>D : Register for storing result (square root value)</div><div>S, D may combine with V, Z, P0~P9 to serve indirect address application</div></div></div> <div><table><tr><th>Range</th><th>HR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td>Ope- rand</td><td>R0 R3839</td><td>R5000 R8071</td><td>D0 D4095</td><td>Floating point number</td><td>V、Z P0~P9</td></tr><tr><td>S</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr><tr><td>D</td><td><input type="radio"/></td><td><input type="radio"/>*</td><td><input type="radio"/></td><td></td><td><input type="radio"/></td></tr></table></div> <div><div>Description</div><div><ul style="list-style-type: none">The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System) page 5-9.When operation control "EN" = 1 or from 0 to 1(P instruction), take the square root of the data specified by the S value or S~S+1 register, and store the result into the register specified by D~D+1.If the value of S is negative, then the error flag "ERR" will be set to 1, and do not execute the operation.<div><div><div>X0</div><div>•</div><div> </div><div> </div><div> </div><div>EN</div></div><div><div>208P.FSQR</div><div>S : 2520.04</div><div>D : D0</div><div>ERR—</div></div></div><div><div>S : <table><tr><td>K</td><td>2520.04</td></tr></table></div><div>↓ X0 = ↑</div><div>D : <table><tr><td>D1</td><td>D0</td><td>50.2</td></tr></table> ⇒ Floating Point Number : <table><tr><td>4248</td><td>CCCD</td><td>H</td></tr><tr><td colspan="2">D1</td><td>D0</td></tr></table></div><div>$\sqrt{2520.04} = 50.2$</div></div></div></div>			Range	HR	ROR	DR	K	XR	Ope- rand	R0 R3839	R5000 R8071	D0 D4095	Floating point number	V、Z P0~P9	S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	D	<input type="radio"/>	<input type="radio"/> *	<input type="radio"/>		<input type="radio"/>	K	2520.04	D1	D0	50.2	4248	CCCD	H	D1		D0
Range	HR	ROR	DR	K	XR																																
Ope- rand	R0 R3839	R5000 R8071	D0 D4095	Floating point number	V、Z P0~P9																																
S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																																
D	<input type="radio"/>	<input type="radio"/> *	<input type="radio"/>		<input type="radio"/>																																
K	2520.04																																				
D1	D0	50.2																																			
4248	CCCD	H																																			
D1		D0																																			

FUN 209 **P**
FSIN

SIN TRIGONOMETRIC INSTRUCTION

FUN 209 **P**
FSIN

Ladder symbol

Operation control — EN

209P.FSIN

S :

D :

ERR — S range error

S : Source register to be taken SIN

D : Register for storing result (SIN value)

S, D may combine with V, Z, P0~P9 to serve indirect address application.

Range	HR	ROR	DR	K	XR
Ope- rand	R0 R3839	R5000 R8071	D0 D4095	Integer 16 Bit number	V · Z P0~P9
S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
D	<input type="radio"/>	<input type="radio"/> *	<input type="radio"/>		<input type="radio"/>

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System) page 5-9.
- When operation control "EN" = 1 or from 0 to 1 (**P** instruction), take the SIN value of the angle data specified by the S register and store the result into the register D~D+1 in floating point number format. The valid range of the angle is from -18000 to +18000, unit in 0.01 degree.
- If the S value is not within the valid range, then the S value error flag "ERR" will be set to 1, and do not execute the operation.

X0

•| |—EN

209P.FSIN

S : 3000

D : R100

ERR—

- At left, the example program gets the SIN value of 30, and stores the results the register DR100.

30

↓
× 100 (bias value)

S

3000

X0 = \int Floating Point number :

DR100

3 F 0 0 0 0 0 0 H

SIN(30) = 0.5

7-164

FUN 210 P FCOS		COS TRIGONOMETRIC INSTRUCTION		FUN 210 P FCOS																								
<div><div>Ladder symbol</div><div><div>210P.FCOS</div><div>S : <div></div></div><div>D : <div></div></div></div><div>Operation control — EN</div><div>ERR — S range error</div></div>		<div>S : Source register to be taken COS</div> <div>D : Register for storing result (COS value)</div> <div>S, D may combine with V, Z, P0~P9 to serve indirect address application</div>																										
<table><tr><th>Range</th><th>HR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td rowspan="2">Ope- rand</td><td>R0 R3839</td><td>R5000 R8071</td><td>D0 D4095</td><td>Integer 16 Bit number</td><td>V、Z P0~P9</td></tr><tr><td>S</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr><tr><td>D</td><td><input type="radio"/></td><td><input type="radio"/>*</td><td><input type="radio"/></td><td></td><td><input type="radio"/></td></tr></table>						Range	HR	ROR	DR	K	XR	Ope- rand	R0 R3839	R5000 R8071	D0 D4095	Integer 16 Bit number	V、Z P0~P9	S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	D	<input type="radio"/>	<input type="radio"/> *	<input type="radio"/>		<input type="radio"/>
Range	HR	ROR	DR	K	XR																							
Ope- rand	R0 R3839	R5000 R8071	D0 D4095	Integer 16 Bit number	V、Z P0~P9																							
	S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																							
D	<input type="radio"/>	<input type="radio"/> *	<input type="radio"/>		<input type="radio"/>																							
<div>Description</div> <div><div><div><div>● The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System) page 5-9.</div><div><div>● When operation control "EN" = 1 or from 0 to 1 (P instruction), take the COS value of the angle data specified by the S register and store the result into the register D~D+1 in floating point number format. The valid range of the angle is from -18000 to +18000, unit in 0.01 degree.</div><div><div>● If the S value is not within the valid range, then the S value error flag "ERR" will be set to 1, and do not execute the operation.</div></div></div><div><div><div><div><div>X0</div><div>• —EN</div><div><div>210P.FCOS</div><div>S : R0</div><div>D : R200</div></div><div>ERR—</div></div><div><div>● At left, the example program gets the COS value of 60, and stores the results the register DR200.</div></div></div><div><div><div><div>60</div><div>↓ × 100 (bias value)</div><div>DR06000</div></div><div>X0 = \int</div><div>Floating Point Number : DR2003F000000H</div></div><div><div>COS(60) = 0.5</div></div></div></div></div></div></div></div>																												

FUN 211 P
FTAN

TAN TRIGONOMETRIC INSTRUCTION

FUN 211 P
FTAN

Ladder symbol

Operation control — EN

211P.FTAN

S :

D :

ERR — S range error

S : Source register to be taken TAN

D : Register for storing result (TAN value)

S, D may combine with V, Z, P0~P9 to serve indirect address application

Range	HR	ROR	DR	K	XR
Ope- rand	R0 R3839	R5000 R8071	D0 D4095	Integer 16 Bit number	V · Z P0~P9
S	<div></div>	<div></div>	<div></div>	<div></div>	<div></div>
D	<div></div>	<div>*</div>	<div></div>		<div></div>

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System) page 5-9.
- When operation control "EN" = 1 or from 0 to 1 (P instruction), take the COS value of the angle data specified by the S register and store the result into the register D~D+1 in floating point number format. The valid range of the angle is from -18000 to +18000, unit in 0.01 degree.
- If the S value is not within the valid range, then the S value error flag "ERR" will be set to 1, and do not execute the operation.

M0

•

—

EN

211P.FTAN

S : R0

D : D50

ERR—

- At left, the example program gets the TAN value of 45, and stores the results the register DD50.

45

↓

× 100 (bias value)

DR0

4500

M0 =

Floating Point Number :

DD50

3F800000H

TAN(45) = 1

FUN 212 P FNEG	CHANGE SIGN OF THE FLOATING POINT NUMBER	FUN 212 P FNEG														
<div><div>Ladder symbol</div><div>Operation control — EN — <div>212P. FNEG<div>D</div></div></div><div>D : Register to be changed sign D may combine with V, Z, P0~P9 to serve indirect address application</div><table><tr><th>Range</th><th>HR</th><th>ROR</th><th>DR</th><th>XR</th></tr><tr><td rowspan="2">Ope- rand</td><td>R0 R3839</td><td>R5000 R8071</td><td>D0 D4095</td><td>V · Z P0~P9</td></tr><tr><td>○</td><td>○*</td><td>○</td><td>○</td></tr></table></div>			Range	HR	ROR	DR	XR	Ope- rand	R0 R3839	R5000 R8071	D0 D4095	V · Z P0~P9	○	○*	○	○
Range	HR	ROR	DR	XR												
Ope- rand	R0 R3839	R5000 R8071	D0 D4095	V · Z P0~P9												
	○	○*	○	○												
<div>Description</div> <ul style="list-style-type: none">● The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System) page 5-9.● When operation control "EN" = 1 or from 0 to 1 (P instruction), the sign of the floating point number register specified by D will be toggled. <div>Programming Example</div> <div><div><div>X0</div><div>— —EN—</div><div>212P. FNEG</div><div>R0</div></div><div>● The instruction at left negates the value of the DR0 register, and stores it back to DR0.</div></div> <div><div><div>DR0</div><div>1 2 3 . 4 5</div></div><div>⇒ Floating Point Number :</div><div><div>DR0</div><div>4 2 F 6 E 6 6 6 H</div></div><div>↓ (NEGATION)</div><div><div>DR0</div><div>- 1 2 3 . 4 5</div></div><div>↓ x0=↗</div><div><div>DR0</div><div>C 2 F 6 E 6 6 6 H</div></div></div>																

FUN 213 **P**
FABS

FLOATING POINT NUMBER ABSOLUTE VALUE

FUN 213 **P**
FABS

Ladder symbol

Operation control — EN —

213P.
FABS

D

D : Register to be taken absolute value

D may combine with V, Z, P0~P9 to serve indirect address application

Range	HR	ROR	DR	XR
Ope- rand	R0 R3839	R5000 R8071	D0 D4095	V · Z P0~P9
	○	○*	○	○
D				

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard. For detail explanation of the format please refer to 5.3 (Numbering System) page 5-9.
- When operation control "EN" = 1 or from 0 to 1 (**P** instruction), calculate the absolute value of the floating point number register specified by D, and write it back into the original D register.

Programming Example

X0

•| | — EN —

213P.
FABS

R0

- The instruction at left calculates the absolute value of the DR0 register, and stores it back in DR0.

DR0 | -1 0 0 . 2 5

⇒ Floating Point Number :

DR0 | C 2 C 8 8 0 0 0 H

↓ (ABSOLUTE)

DR0 | 1 0 0 . 2 5

↓ x0 = ⌈

DR0 | 4 2 C 8 8 0 0 0 H

Floating Point Instructions

FUN 214 P FLN	FLOATING POINT NAPIERIAN LOGARITHM, $\log_e x$ or $\ln(x)$	FUN 214 P FLN
-------------------------	---	-------------------------

Operation Control EN

F214P.FLN
 S :
 D :

ERR

S : Source data or register to be calculated Napierian logarithm value

D : Register for storing the result

S, D may combine with V, Z, P0~P9 to serve indirect address application

Range	HR	ROR	DR	K	XR
Ope- rand	R0 R3839	R5000 R8071	D0 D3999	Floating number	V · Z P0 ~ P9
	S	○	○	○	○
D	○	○*	○		○

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard of 32-bit.
- When operation control "EN" = 1 or from 0 to 1 (**P** instruction), take the Napierian logarithm of the data specified by the S value or S~S+1 register, and store the result into the register specified by D~D+1.
- If the value of S is negative or equal to 0 、 invalid indirect addressing 、 or over range of the result , the error flag "ERR" will be set to 1, and not update the value of D~D+1.
- All floating point instructions can't be executed in interrupt service routine.

Example

- When M214=1, calculate the Napierian logarithm value, it is DD246 = ln (DD46)

FUN 215 P
FEXP

FLOATING POINT NATURE POWER FUNCTION, e^x

FUN 215 P
FEXP

Operation Control EN

F215P.FEXP

S :
D :

ERR

S : Source data or register to be calculated power function of nature number

D : Register for storing the result

S, D may combine with V, Z, P0~P9 to serve indirect address application

Range	HR	ROR	DR	K	XR
Ope- rand	R0 R3839	R5000 R8071	D0 D3999	Floating number	V · Z P0~P9
S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
D	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>		<input type="radio"/>

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard of 32-bit.
- When operation control "EN" = 1 or from 0 to 1 (P instruction), calculate the nature power function of the data specified by the S value or S~S+1 register, and store the result into the register specified by D~D+1.
- If the value of S is out of range、invalid indirect addressing、or over range of the result , the error flag "ERR" will be set to 1, and not update the value of D~D+1.
- All floating point instructions can't be executed in interrupt service routine.

Example

N0L7

M215

EN

215.FEXP

S :
D :

ERR

M520

S : D48
-0.123

D : D248
0.88426363

- When M215=1, calculate the nature power function, it is DD248 = e^{DD48}

Status Monitoring

Ref. No.	Status	Data	Ref. No.	Status	Data	F
DD48	Floating	-0.123				
DD248	Floating	0.88426363				
M215	Enable	ON				

StatusPage2 / StatusPage1

FUN 216 P
FLOG

FLOATING POINT LOGARITHM, log₁₀X or log(x)

FUN 216 P
FLOG

Operation Control EN

F216P.FLOG

S :

D :

ERR

S : Source data or register to be calculated logarithm value

D : Register for storing the result

S, D may combine with V, Z, P0~P9 to serve indirect address application

Range	HR	ROR	DR	K	XR
Ope-rand	R0 R3839	R5000 R8071	D0 D3999	Floating number	V · Z P0~P9
S	○	○	○	○	○
D	○	○*	○		○

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard of 32-bit.
- When operation control "EN" = 1 or from 0 to 1 (P instruction), calculate the logarithm value of the data specified by the S value or S~S+1 register, and store the result into the register specified by D~D+1.
- If the value of S is negative or equal to 0 、 invalid indirect addressing 、 or over range of the result , the error flag "ERR" will be set to 1, and not update the value of D~D+1.
- All floating point instructions can't be executed in interrupt service routine.

Example

N019

M216

EN

216.FLOG

S : 050
0.123

D : D250
-0.91009486

ERR

M521

- When M216=1, calculate the logarithm value, it is DD250 = log (DD50)

Status Monitoring

Ref. No.	Status	Data	Ref. No.	Status	Data	F
DD50	Floating	0.123				
DD250	Floating	-0.91009486				
M216	Enable	ON				

StatusPage2 / StatusPage1

FUN 217 P
FPOW

FLOATING POINT POWER FUNCTION, x^y

FUN 217 P
FPOW

Operation Control EN

F217P.FPOW

Sy :
Sx :
D :

ERR

Sy: Source data or register of exponential

SX: Source data or register of base °

D : Register for storing the result

Sy, Sx, D may combine with V, Z, P0~P9 to serve indirect address application

Range	HR	ROR	DR	K	XR
Ope- rand	R0 R3839	R5000 R8071	D0 D3999	Floating number	V · Z P0~P9
	Sy	○	○	○	○
Sx	○	○*	○	○	○
D	○	○	○		○

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard of 32-bit.
- When operation control "EN" = 1 or from 0 to 1 (P instruction), calculate the power function of the exponential data specified by the Sy 、 base data specified by the Sx, and store the result into the register specified by D~D+1.
- If it exists invalid indirect addressing 、 or over range of the result , the error flag "ERR" will be set to 1, and not update the value of D~D+1.
- All floating point instructions can't be executed in interrupt service routine.

Example

NO21

M217

EN

217.FPOW

Sy: 052
12.34

Sx: 054
99.900002

D : 0252
4.7276013e+24

ERR { }

- When M217=1, calculate the power function, it is DD252 = DD54^{DD52}

Status Monitoring

Ref. No.	Status	Data	Ref. No.	Status	Data	F
DD52	Floating	12.34				
DD54	Floating	99.900002				
DD252	Floating	4.7276013e+24				
M217	Enable	ON				

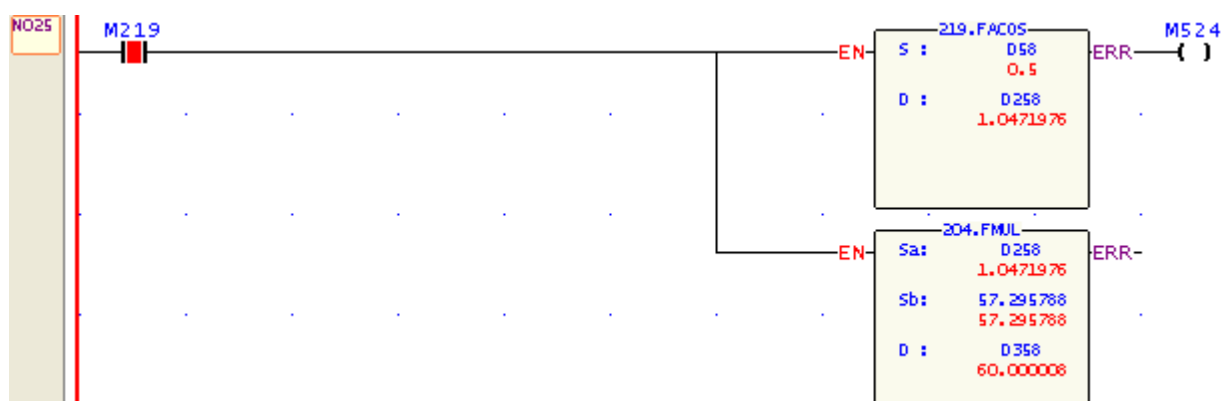
FUN 218 P FASIN	FLOATING POINT ARC SINE FUNCTION, \sin^{-1}	FUN 218 P FASIN																																			
<div><div>Operation Control EN</div><div><div>F218P.FASIN</div><div>S : D :</div></div><div>ERR</div></div> <div><div>S : Source data or register to be calculated the arc sine value</div><div>D : Register for storing the result</div><div>S, D may combine with V, Z, P0~P9 to serve indirect address application</div></div> <table><tr><th>Range</th><th>HR</th><th>ROR</th><th>DR</th><th>K</th><th>XR</th></tr><tr><td rowspan="2">Ope- rand</td><td>R0 R3839</td><td>R5000 R8071</td><td>D0 D3999</td><td>Floating number</td><td>V · Z P0~P9</td></tr><tr><td>S</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr><tr><td>D</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input checked="" type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr></table>			Range	HR	ROR	DR	K	XR	Ope- rand	R0 R3839	R5000 R8071	D0 D3999	Floating number	V · Z P0~P9	S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	D	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>												
Range	HR	ROR	DR	K	XR																																
Ope- rand	R0 R3839	R5000 R8071	D0 D3999	Floating number	V · Z P0~P9																																
	S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>																																
D	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>																																
<div>Description</div> <div><div><div>The format of floating point number of Fatek-PLC follows the IEEE-754 standard of 32-bit.</div><div>When operation control "EN" = 1 or from 0 to 1 (P instruction), calculate the arc sine value of the data specified by the S value or S~S+1 register, and store the result into the register specified by D~D+1.</div><div>Range of S data : -1~ +1 ; range of D value : $-\pi/2 \sim \pi/2$ (Unit in radian)</div><div>If the value of S is out of range \ or invalid indirect addressing, the error flag "ERR" will be set to 1, and not update the value of D~D+1.</div><div>All floating point instructions can't be executed in interrupt service routine.</div></div></div> <div><div>Example</div><div><div><div><div>NO23</div><div>M218</div></div><div><div>218.FASIN</div><div>S : D56 0.70710677</div><div>D : D256 0.78539813</div><div>ERR → M523</div></div><div><div>204.FMUL</div><div>Sa: D256 0.78539813</div><div>Sb: 57.295788 57.295788</div><div>D : D356 45.000004</div><div>ERR →</div></div></div></div><div><div>When M218=1, calculate the arc sine value, it is DD256 = \sin^{-1} DD56; DD256(Unit in radian) × 57.295788(180/ π) to acquire the degree value</div></div><div><div>Status Monitoring</div><table><tr><th>Ref. No.</th><th>Status</th><th>Data</th><th>Ref. No.</th><th>Status</th><th>Data</th><th>F</th></tr><tr><td>DD56</td><td>Floating</td><td>0.70710677</td><td></td><td></td><td></td><td></td></tr><tr><td>DD256</td><td>Floating</td><td>0.78539813</td><td></td><td></td><td></td><td></td></tr><tr><td>M218</td><td>Enable</td><td>ON</td><td></td><td></td><td></td><td></td></tr><tr><td>DD356</td><td>Floating</td><td>45.000004</td><td></td><td></td><td></td><td></td></tr></table></div></div>			Ref. No.	Status	Data	Ref. No.	Status	Data	F	DD56	Floating	0.70710677					DD256	Floating	0.78539813					M218	Enable	ON					DD356	Floating	45.000004				
Ref. No.	Status	Data	Ref. No.	Status	Data	F																															
DD56	Floating	0.70710677																																			
DD256	Floating	0.78539813																																			
M218	Enable	ON																																			
DD356	Floating	45.000004																																			

FUN 219 P FACOS	FLOATING POINT ARC COSINE FUNCTION, \cos^{-1}	FUN 219 P FACOS																		
<div><div>Operation Control EN</div><div><div>F219P.FACOS</div><div>S : D :</div></div><div>ERR</div></div> <div><div>S : Source data or register to be calculated the arc cosine value</div><div>D : Register for storing the result</div><div>S, D may combine with V, Z, P0~P9 to serve indirect address application</div></div>																				
<table><tr><th>Range Ope- rand</th><th>HR R0 R3839</th><th>ROR R5000 R8071</th><th>DR D0 D3999</th><th>K Floating number</th><th>XR V、Z P0~P9</th></tr><tr><td>S</td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr><tr><td>D</td><td><input type="radio"/></td><td><input type="radio"/>*</td><td><input type="radio"/></td><td></td><td><input type="radio"/></td></tr></table>			Range Ope- rand	HR R0 R3839	ROR R5000 R8071	DR D0 D3999	K Floating number	XR V、Z P0~P9	S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	D	<input type="radio"/>	<input type="radio"/> *	<input type="radio"/>		<input type="radio"/>
Range Ope- rand	HR R0 R3839	ROR R5000 R8071	DR D0 D3999	K Floating number	XR V、Z P0~P9															
S	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>															
D	<input type="radio"/>	<input type="radio"/> *	<input type="radio"/>		<input type="radio"/>															

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard of 32-bit.
- When operation control "EN" = 1 or from 0 to 1 (**P** instruction), calculate the arc cosine value of the data specified by the S value or S~S+1 register, and store the result into the register specified by D~D+1.
- Range of S data : -1~ +1 ; range of D value : 0 ~ π (Unit in radian)
- If the value of S is out of range or invalid indirect addressing, the error flag "ERR" will be set to 1, and not update the value of D~D+1.
- All floating point instructions can't be executed in interrupt service routine.

Example



- When M219=1, calculate the arc cosine value, it is DD258 = \cos^{-1} DD58;
DD258(Unit in radian) \times 57.295788($180/\pi$) to acquire the degree value

Status Monitoring					
Ref. No.	Status	Data	Ref. No.	Status	Data
DD58	Floating	0.5			
DD258	Floating	1.0471976			
M219	Enable	ON			
DD358	Floating	60.000008			

FUN 220 P FATAN	FLOATING POINT ARC TANGENT FUNCTION, \tan^{-1}	FUN 220 P FATAN
----------------------------------	--	----------------------------------

Operation Control EN

F220P.FATAN

S :

D :

S : Source data or register to be calculated the arc tangent value

D : Register for storing the result

S, D may combine with V, Z, P0~P9 to serve indirect address application

Range	HR	ROR	DR	K	XR
Ope- rand	R0	R5000	D0	Floating number	V · Z P0~P9
	R3839	R8071	D3999		
S	○	○	○	○	○
D	○	○*	○	○	○

Description

- The format of floating point number of Fatek-PLC follows the IEEE-754 standard of 32-bit.
- When operation control "EN" = 1 or from 0 to 1 (**P** instruction), calculate the arc tangent value of the data specified by the S value or S~S+1 register, and store the result into the register specified by D~D+1.
- S data is any number ; range of D value : $-\pi/2 \sim \pi/2$ (Unit in radian)
- If it exists invalid indirect addressing, the error flag "ERR" will be set to 1, and not update the value of D~D+1.
- All floating point instructions can't be executed in interrupt service routine.

Example

- When M220=1, calculate the arc tangent value, it is DD260 = \tan^{-1} DD60;
DD260(Unit in radian) × 57.295788(180/π) to acquire the degree value

Status Monitoring

_
□
✕

Ref. No.	Status	Data	Ref. No.	Status	Data	F
DD60	Floating	1.23				
DD260	Floating	0.88817382				
M220	Enable	ON				
DD360	Floating	50.888618				

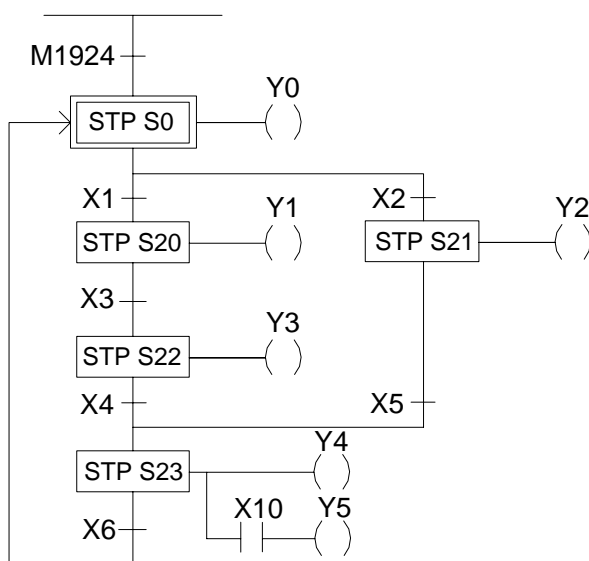
Chapter 8 Step Instruction Description

Structured programming design is a major trend in software design. The benefits are high readability, easy maintenance, convenient updating and high quality and reliability. For the control applications, consisted of many sequential tasks, designed by conventional ladder program design methodology usually makes others hard to maintain. Therefore, it is necessary to combine the current widely used ladder diagrams with the sequential controls made especially for machine working flow. With help from step instructions, the design work will become more efficient, time saving and controlled. This kind of design method that combines process control and ladder diagram together is called the step ladder language.

The basic unit of step ladder diagram is a step. A step is equivalent to a movement (step) in the machine operation where each movement has an output. The complete machine or the overall sequential control process is the combination of steps in serial or parallel. Its step-by-step sequential execution procedure allows others to be able to understand the machine operations thoroughly, so that design, operation, and maintenance will become more effective and simpler.

8.1 The Operation Principle of Step Ladder Diagram

【Example】



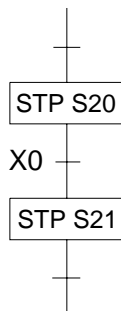
【Description】

1. **STP Sxxx** is the symbol representing a step Sxxx that can be one of S0 ~ S999. When executing the step (status ON), the ladder diagram on the right will be executed and the previous step and output will become OFF.
2. M1924 is on for a scan time after program start. Hence, as soon as ON, the stop of the initial step S0 is entered (S0 ON) while the other steps are kept inactive, i.e. Y1~Y5 are all OFF. This means M1924 ON→S0 ON→Y0 ON and Y0 will remain ON until one of the contacts X1 or X2 is ON.
3. Assume that X2 is ON first; the path to S21 will then be executed.

$$X2 \text{ ON} \Rightarrow \begin{cases} S21 \text{ ON} \\ S0 \text{ OFF} \end{cases} \Rightarrow \begin{cases} Y2 \text{ ON} \\ Y0 \text{ OFF} \end{cases}$$
 Y2 will remain ON until X5 is ON.
4. Assume that X5 is ON, the process will move forward to step S23.
 i.e. $X5 \text{ ON} \Rightarrow \begin{cases} S23 \text{ ON} \\ S21 \text{ OFF} \end{cases} \Rightarrow \begin{cases} Y4 \text{ ON} \\ Y2 \text{ OFF} \end{cases}$
 Y4 and Y5 will remain ON until X6 is ON.
 ※If X10 is ON, then Y5 will be ON.
5. Assume that X6 is ON, the process will move forward to S0.
 i.e. $X6 \text{ ON} \Rightarrow \begin{cases} S0 \text{ ON} \\ S23 \text{ OFF} \end{cases} \Rightarrow \begin{cases} Y0 \text{ ON} \\ Y4, Y5 \text{ OFF} \end{cases}$
 Then, a control process cycle is completed and the next control process cycle is entered.

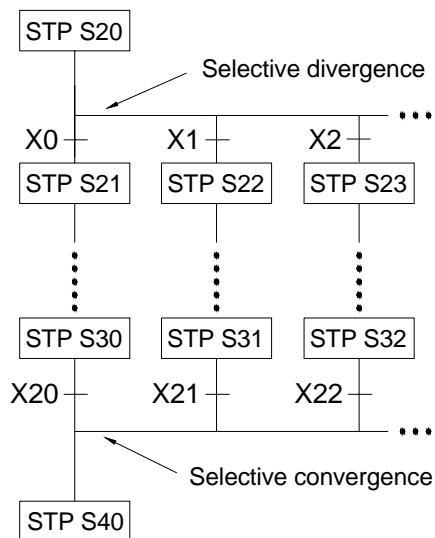
8.2 Basic Formation of Step Ladder Diagram

① Single path



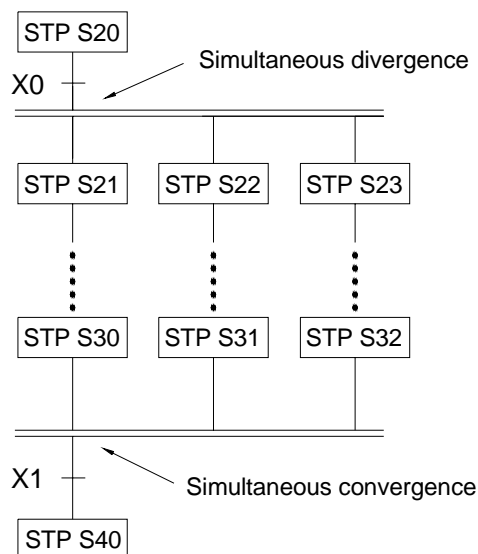
- Step S20 alone moves to step S21 through X0.
- X0 can be changed to other serial or parallel combination of contacts.

② Selective divergence/convergence



- Step S20 selects an only one path which divergent condition first met. E.g. X2 is ON first, then only the path of step S23 will be executed.
- A divergence may have up to 8 paths maximum.
- X1, X2,, X22 can all be replaced by the serial or parallel combination of other contacts.

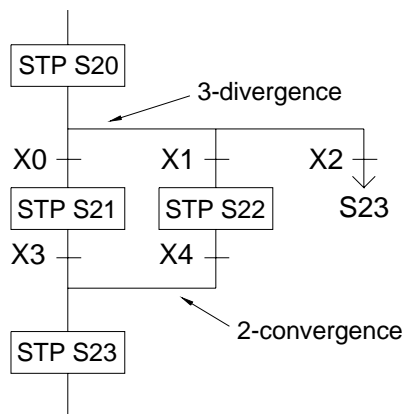
③ Simultaneous divergence/convergence



- After X0 is ON, step S20 will simultaneously execute all paths below it, i.e. all S21, S22, S23, and so on, are in action.
- All divergent paths at a convergent point will be executed to the last step (e.g. S30, S31 and S32). When X1 is ON, they can then transfer to S40 for execution.
- The number of divergent paths must be the same as the number of convergent paths. The maximum number of divergence/convergence path is 8.

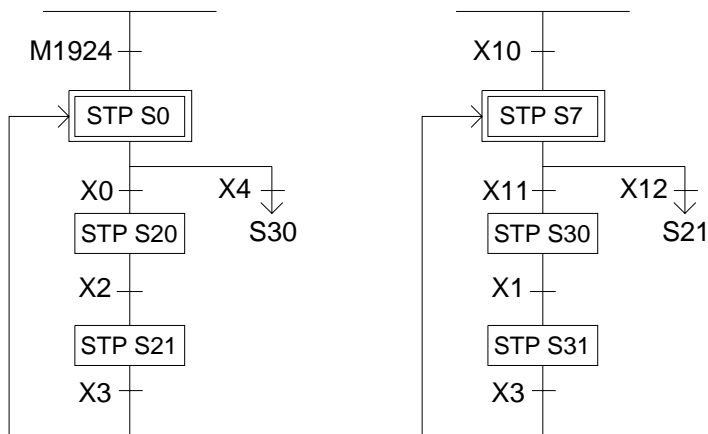
④ Jump

a. The same step loop



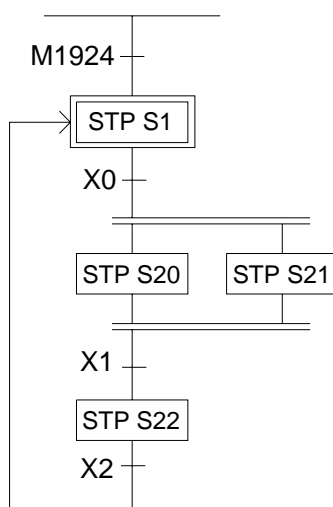
- There are 3 paths below step S20 as shown on the left. Assume that X2 is ON, then the process can jump directly to step S23 to execute without going through the process of selective convergence.
- The execution of simultaneous divergent paths can not be skipped.

b. Different step loop

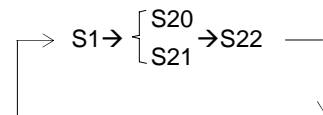


⑤ Closed Loop and Single Cycle

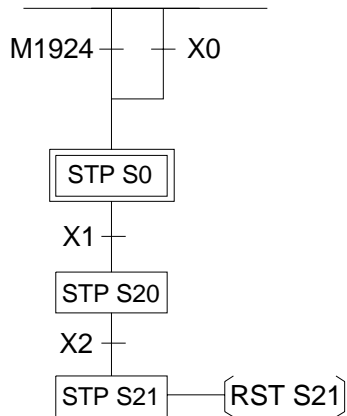
a. Closed Loop



- The initial step S1 is ON, endless cycle will be continued afterwards.

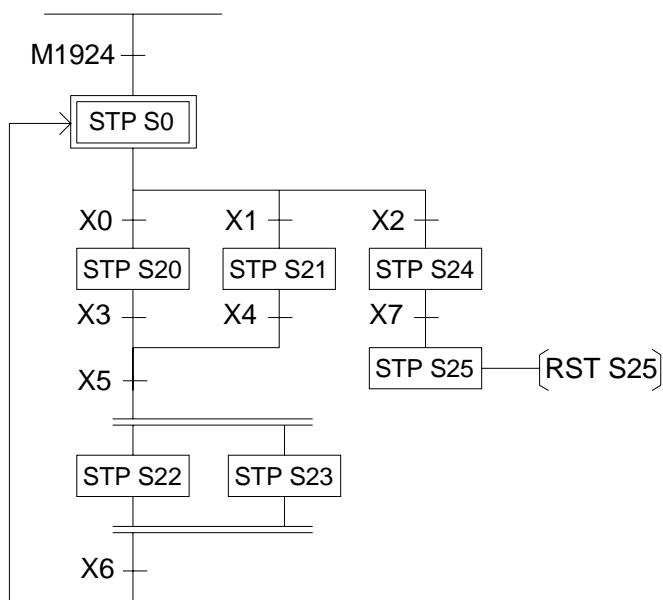


b. Single Cycle

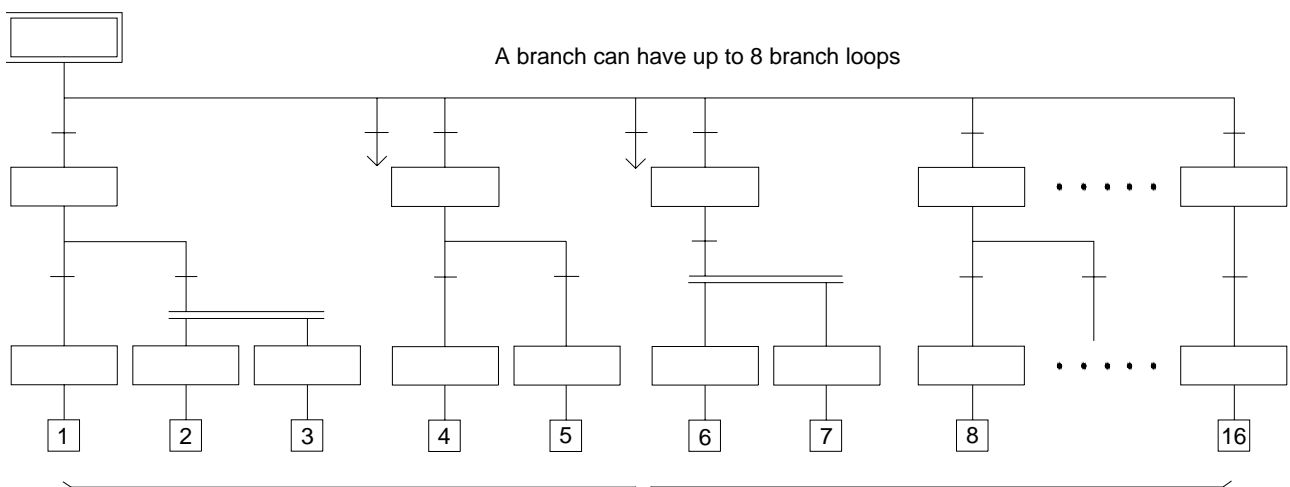


- When step S20 is ON, if X2 is also ON, then “RST S21” instruction will let S21 OFF which will stop the whole step process.

c. Mixed Process



⑥ Combined Application



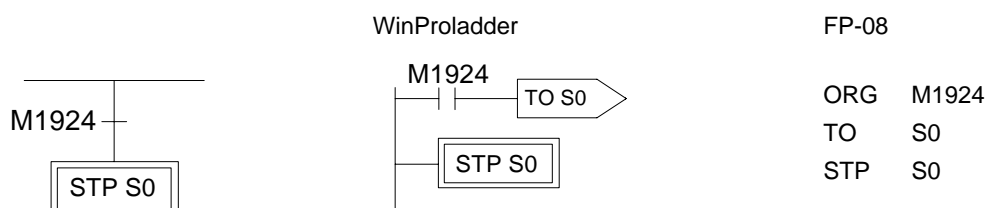
The maximum number of downward horizontal branch loops of an initial step is 16

8.3 Introduction of Step Instructions: STP, FROM, TO and STPEND

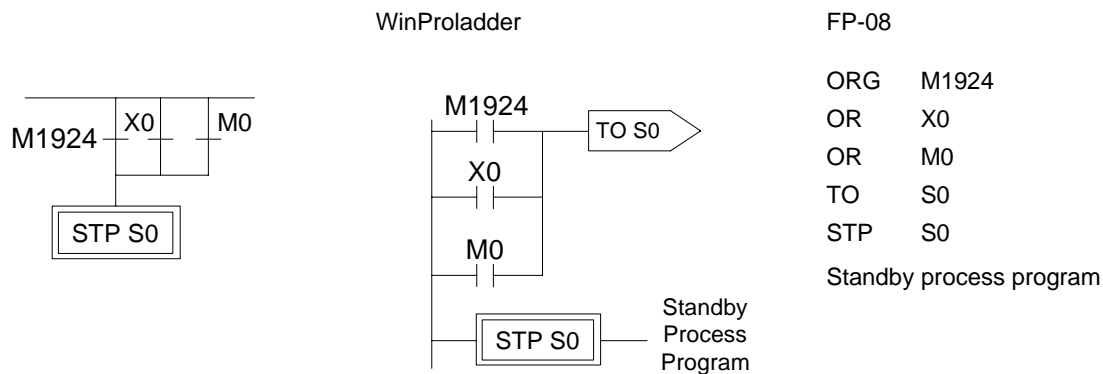
- **STP Sx** : $S0 \leq Sx \leq S7$ (Displayed in WinProladder)
or
STP Sx : $S0 \leq Sx \leq S7$ (Displayed in FP-08)

This instruction is the initial step instruction from where the step control of each machine process can be derived. Up to 8 initial steps can be used in the FBs series, i.e. a PLC can make up to 8 process controls simultaneously. Each step process can operate independently or generate results for the reference of other processes.

【Example 1】 Go to the initial step S0 after each start (ON)



【Example 2】 Each time the device is start to run or the manual button is pressed or the device is malfunction, then the device automatically enters the initial step S0 to standby.



【Description】 X0: Manual Button, M0: Abnormal Contact.

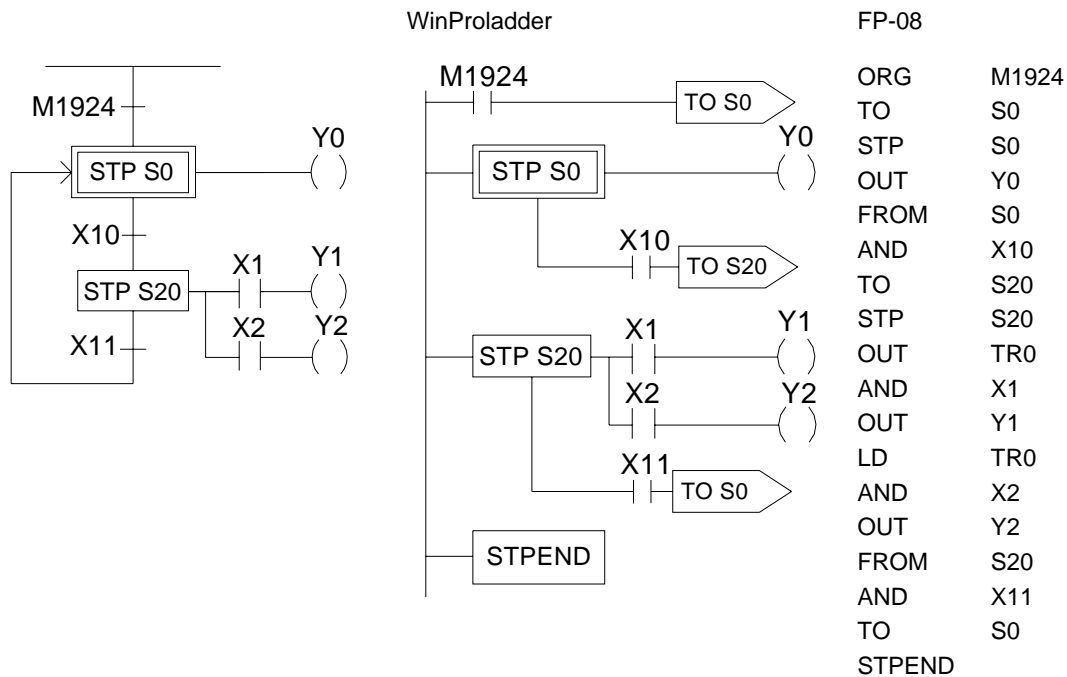
● **STP Sxxx** : $S20 \leq Sxxx \leq S999$ (Displayed in WinProladder)

or

STP Sxxx : $S20 \leq Sxxx \leq S999$ (Displayed in FP-08)

This instruction is a step instruction, each step in a process represents a step of sequence. If the status of step is ON then the step is active and will execute the ladder program associate to the step.

【Example】



【Description】 1. When ON, the initial step S0 is ON and Y0 is ON.

2. When transfer condition X10 is ON (in actual application, the transferring condition may be formed by the serial or parallel combination of the contacts X, Y, M, T and C), the step S20 is activated. The system will automatically turn S0 OFF in the current scan cycle and Y0 will be reset automatically to OFF.

$$\text{i.e. } X10 \text{ ON} \Rightarrow \begin{cases} S20 \text{ ON} \\ S0 \text{ OFF} \end{cases} \Rightarrow \begin{cases} X1 \text{ ON} \rightarrow Y1 \text{ ON} \\ X2 \text{ ON} \rightarrow Y2 \text{ ON} \\ Y0 \text{ OFF} \end{cases}$$

3. When the transfer condition X11 is ON, the step S0 is ON, Y0 is ON and S20, Y1 and Y2 will turn OFF at the same time.

$$\text{i.e. } X11 \text{ ON} \Rightarrow \begin{cases} S0 \text{ ON} \\ S20 \text{ OFF} \end{cases} \Rightarrow \begin{cases} Y0 \text{ ON} \\ Y1 \text{ OFF} \\ Y2 \text{ OFF} \end{cases}$$

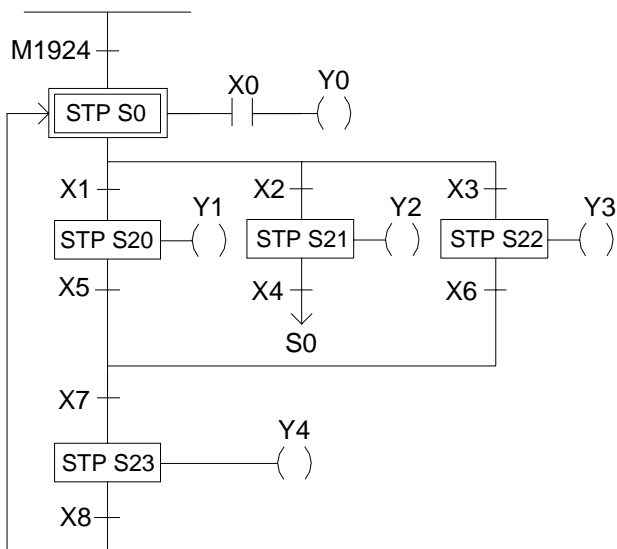
● FROM Sxxx : $S0 \leq Sxxx \leq S999$ (Displayed in WinProladder)

or

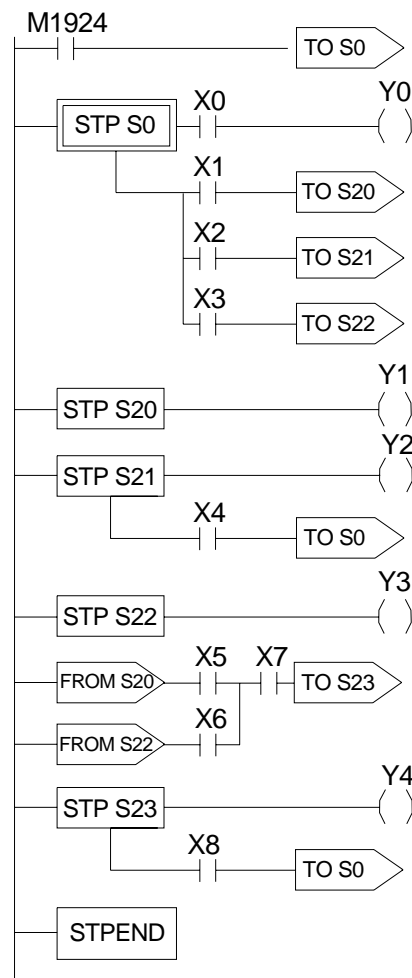
FROM Sxxx : $S0 \leq Sxxx \leq S999$ (Displayed in FP-08)

The instruction describes the source step of the transfer, i.e. moving from step Sxxx to the next step in coordination with transfer condition.

【Example】



WinProladder



FP-08

```

ORG      M1924
TO       S0
STP      S0
AND      X0
OUT      Y0
FROM     S0
OUT TR   0
AND      X1
TO       S20
LD TR    0
AND      X2
TO       S21
LD TR    0
AND      X3
TO       S22
LD TR    0
AND      X4
TO       S0
STP      S20
OUT      Y1
STP      S21
OUT      Y2
FROM     S21
AND      X4
TO       S0
STP      S22
OUT      Y3
FROM     S20
AND      X5
FROM     S22
AND      X6
ORLD
AND      X7
TO       S23
STP      S23
OUT      Y4
FROM     S23
AND      X8
TO       S0
STPEND

```


- 【Description】 : 1. When ON, the initial step S0 is ON. If X0 is ON, then Y0 will be ON.
2. When S0 is ON: a. if X1 is ON, then step S20 will be ON and Y1 will be ON.
b. if X2 is ON, then step S21 will be ON and Y2 will be ON.
c. if X3 is ON, then step S22 will be ON and Y3 will be ON.
d. if X1, X2 and X3 are all ON simultaneous, then step S20 will have the priority to be ON first and either S21 or S22 will not be ON.
e. if X2 and X3 are ON at the same time, then step S21 will have the priority to be ON first and S22 will not be ON.
3. When S20 is ON, if X5 and X7 are ON at the same time, then step S23 will be ON, Y4 will be ON and S20 and Y1 will be OFF.
4. When S21 is ON, if X4 is ON, then step S0 will be ON and S21 and Y2 will be OFF.
5. When S22 is ON, if X6 and X7 are ON at the same time, then step S23 will be ON, Y4 will be ON and S22 and Y3 will be OFF.
6. When S23 is ON, if X8 is ON, then step S0 will be ON and S23 and Y4 will be OFF.

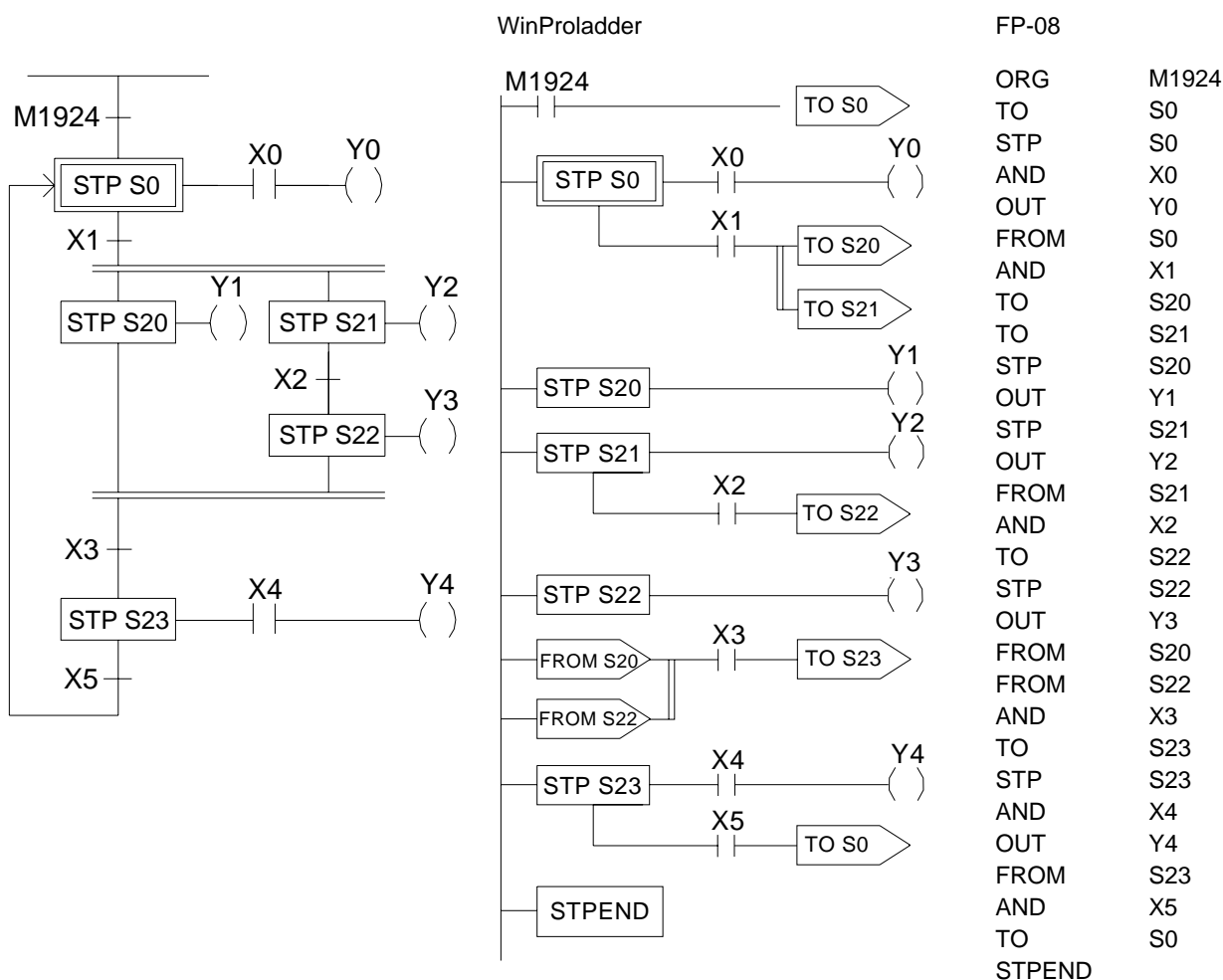
● **TO Sxxx** : $S0 \leq Sxxx \leq S999$ (Displayed in WinProladder)

or

TO Sxxx : $S0 \leq Sxxx \leq S999$ (Displayed in FP-08)

This instruction describes the step to be transferred to.

【Example】



【Description】 : 1. When ON, the initial step S0 is ON. If X0 is ON, then Y0 will be ON.

- When S0 is ON: if X1 is ON, then steps S20 and S21 will be ON simultaneously and Y1 and Y2 will also be ON.
- When S21 is ON: if X2 is ON, then step S22 will be ON, Y3 will be ON and S21 and Y2 will be OFF.
- When S20 and S22 are ON at the same time and the transferring condition X3 is ON, then step S23 will be ON (if X4 is ON, then Y4 will be ON) and S20 and S22 will automatically turn OFF and Y1 and Y3 will also turn OFF.
- When S23 is ON: if X5 is ON, then the process will transfer back to the initial step, i.e. S0 will be ON and S23 and Y4 will be OFF.

● **STPEND** : (Displayed in WinProladder)

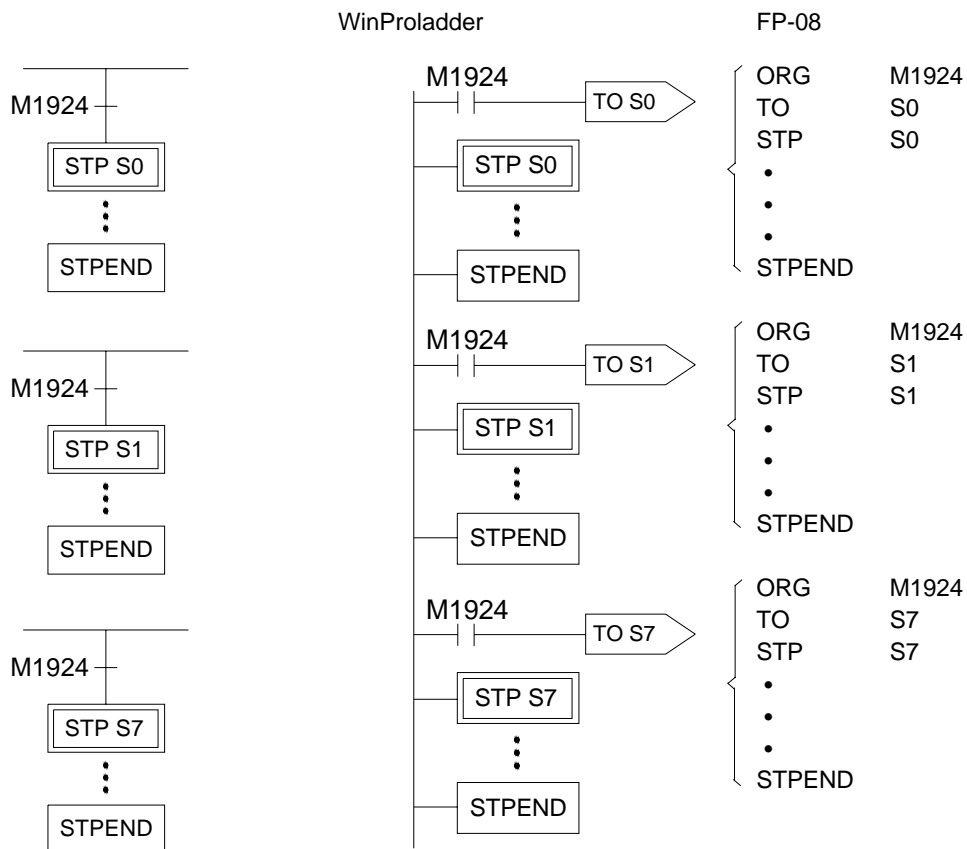
or

STPEND : (Displayed in FP-08)

This instruction represents the end of a process. It is necessary to include this instruction so all processes can be operated correctly.

A PLC can have up to 8 step processes (S0~S7) and is able to control them simultaneously. Therefore, up to 8 STPEND instructions can be obtained.

【Example】

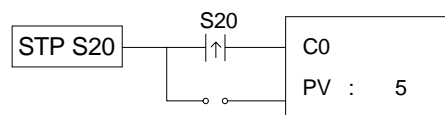


【Description】 When ON, the 8 step processes will be active simultaneously.

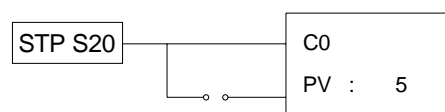
8.4 Notes for Writing a Step Ladder Diagram

【Notes】

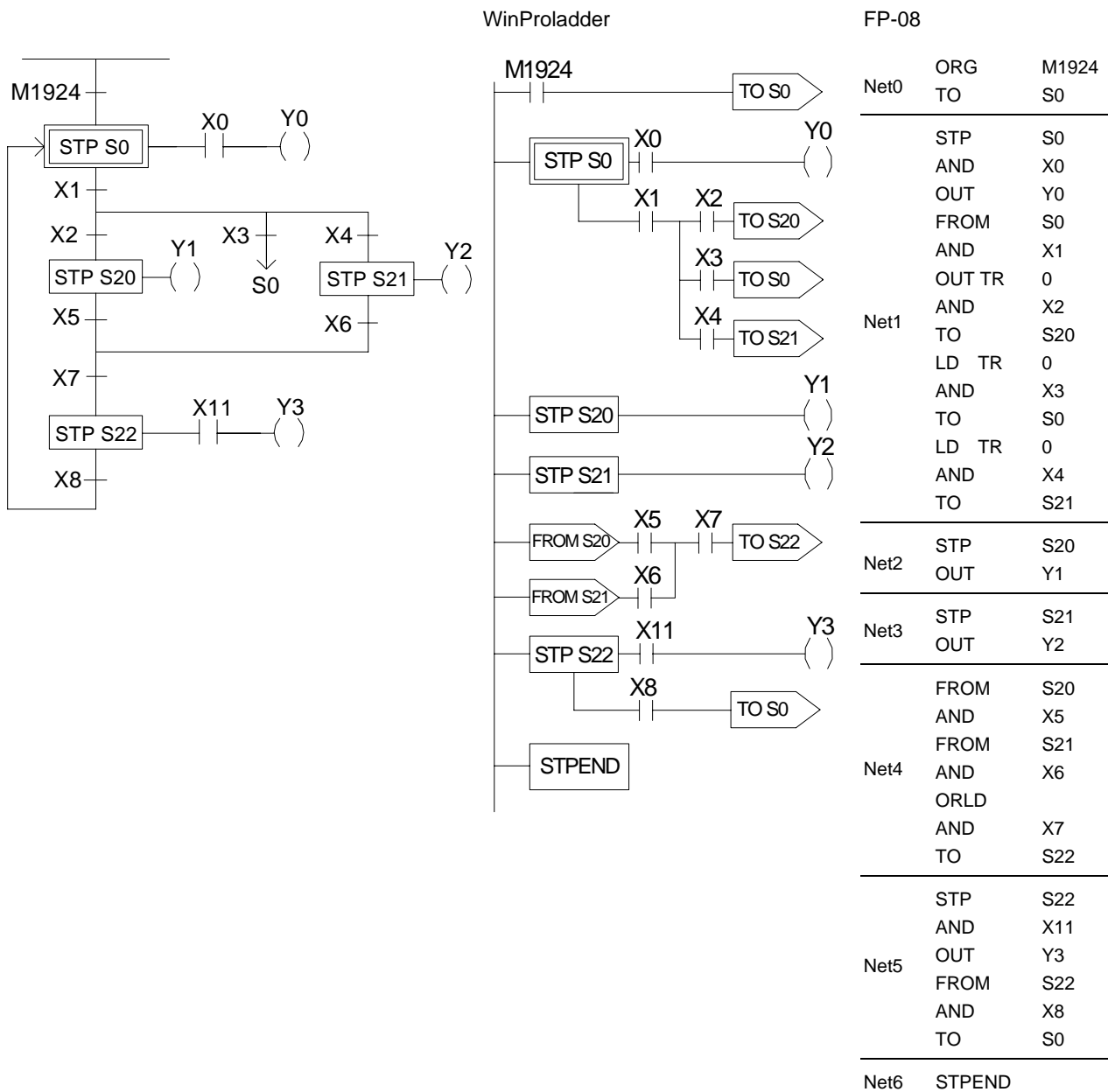
- In actual applications, the ladder diagram can be used together with the step ladder.
- There are 8 steps, S0~S7, that can be used as the starting point and are called the “initial steps”.
- When PLC starts operating, it is necessary to activate the initial step. The M1924 (the first scan ON signal) provided by the system may be used to activate the initial step.
- Except the initial step, the start of any other steps must be driven by other step.
- It is necessary to have an initial step and the final STPEND instruction in a step ladder diagram to complete a step process program.
- There are 980 steps, S20~S999, available that can be used freely. However, used numbers cannot be repeated. S500~S999 are retentive(The range can be modified by users), can be used if it is required to continue the machine process after power is off.
- Basically a step must consists of three parts which are control output, transition conditions and transition targets.
- MC and SKP instructions cannot be used in a step program and the sub-programs. It's recommended that JMP instruction should be avoided as much as possible.
- If the output point is required to stay ON after the step is divergent to other step, it is necessary to use the SET instruction to control the output point and use RST instruction to clear the output point to OFF.
- Looking down from an initial step, the maximum number of horizontal paths is 16. However, a step is only allowed to have up to 8 branch paths.
- When M1918=0 (default) , if a PULSE type function instruction is used in master control loop (FUN 0) or a step program, it is necessary to connect a TU instruction before the function instruction. For example,



When M1918=1, the TU instruction is not required, e.g.:



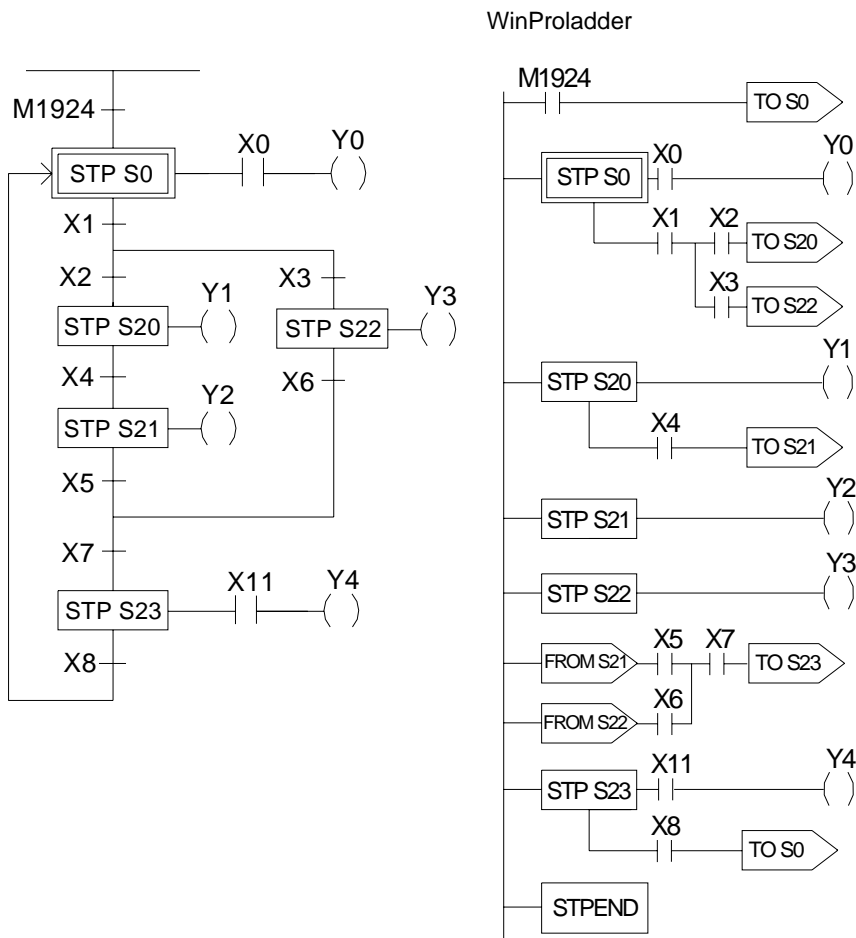
Example 1



Description

1. Input the condition to initial step S0
2. Input the S0 and the divergent conditions of S20, S0 and S21
3. Input the S20
4. Input the S21
5. Input the convergence of S20 and S21
6. Input the S22

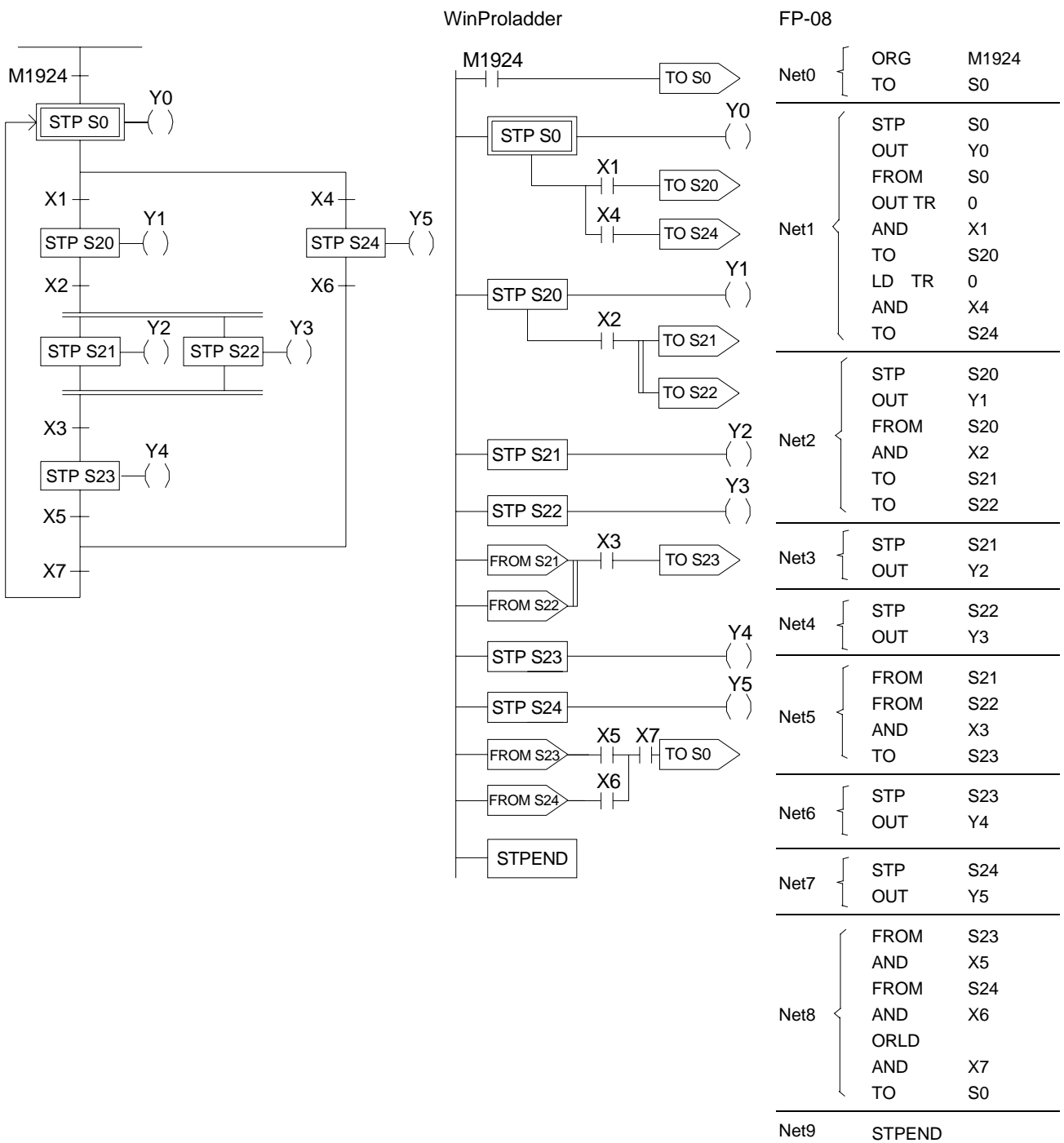
Example 2



Description

1. Input the condition to initial step S0
2. Input the S0 and the divergent condition of S20 and S22
3. Input the S20
4. Input the S21
5. Input the S22
6. Input the convergence of S21 and S22
7. Input the S23

Example 3

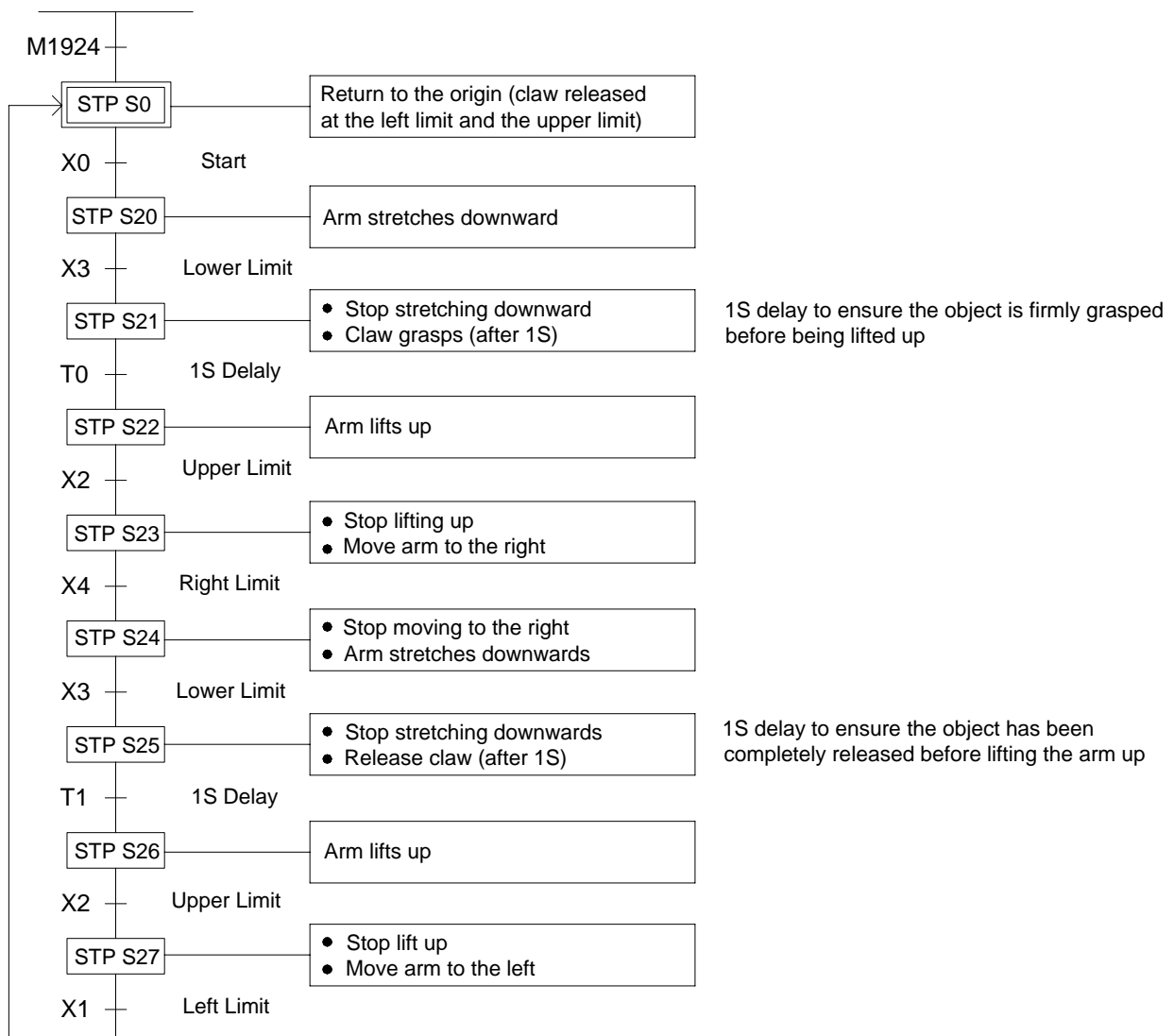
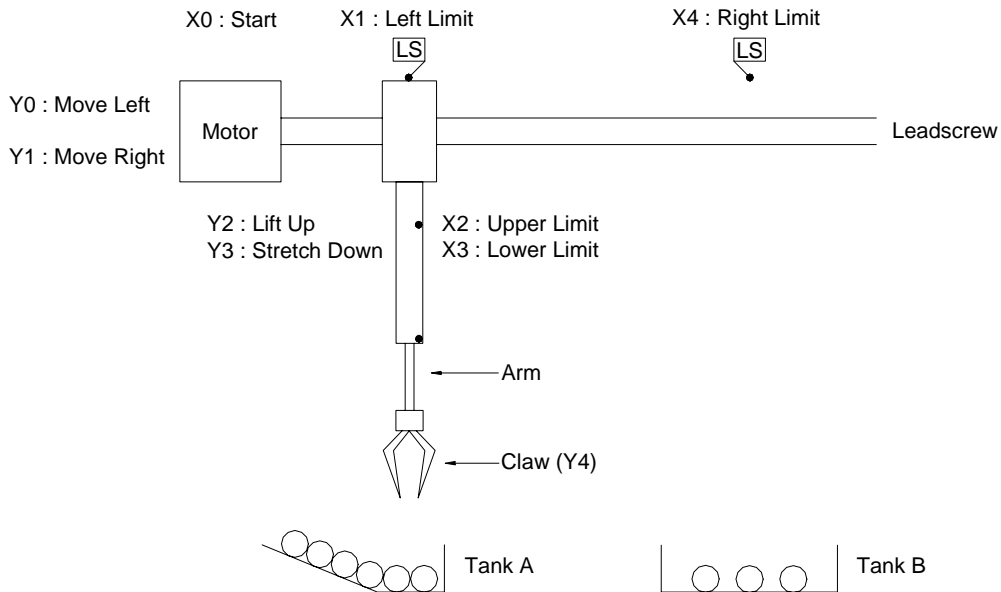


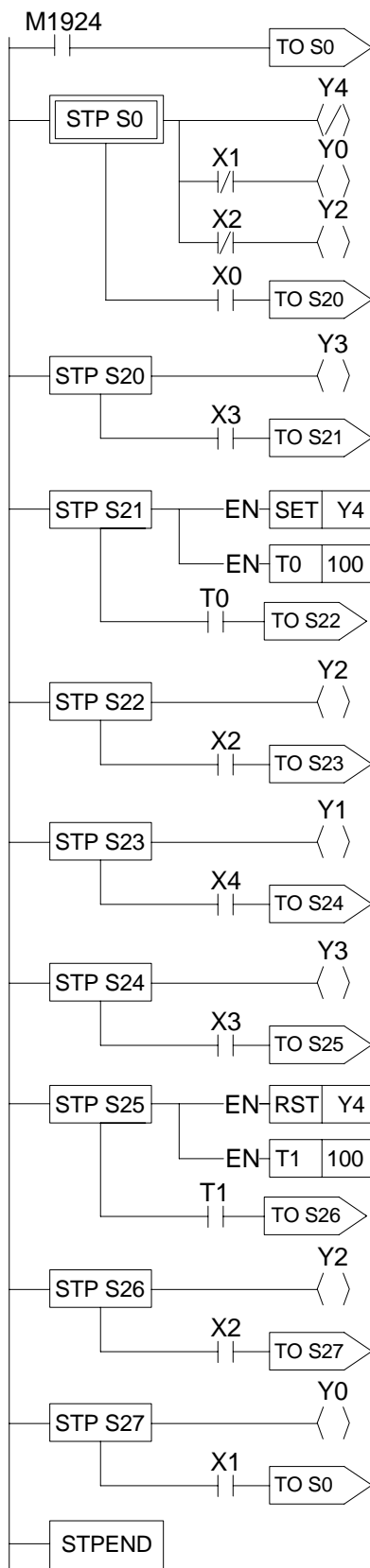
Description

1. Input the condition to initial step S_0
2. Input the S_0 and the divergences of S_{20} and S_{24}
3. Input the S_{20}
4. Input the S_{20} and the divergences of S_{21} and S_{22}
5. Input the S_{21}
6. Input the S_{22}
7. Input the convergences of S_{21} and S_{22}
8. Input the S_{23}
9. Input the S_{24}
10. Input the convergences of S_{23} and S_{24}

8.5 Application Examples

Example 1 Grasp an object from tank A and put it in Tank B





Release claw

Return to the left limit

Return to the upper limit

Turn the switch ON before moving to S20

Stretch arm downward

Move to S21 after stretching to the lower limit

Claw grasps (since the SET instruction is used, Y4 should remain ON after departing from STP S21)

Divergent into S22 after 1S

Lift the arm up

Divergent into S23 after reaching the upper limit

Move arm to the right

Divergent into S24 after moving to the right limit

Stretch the arm downward

Divergent into S25 after stretching to the lower limit

Release claw

Delay for 1S

Transfer into S26 after 1S

Lift the arm up

Divergent into S27 after reaching the upper limit

Move the arm to the left

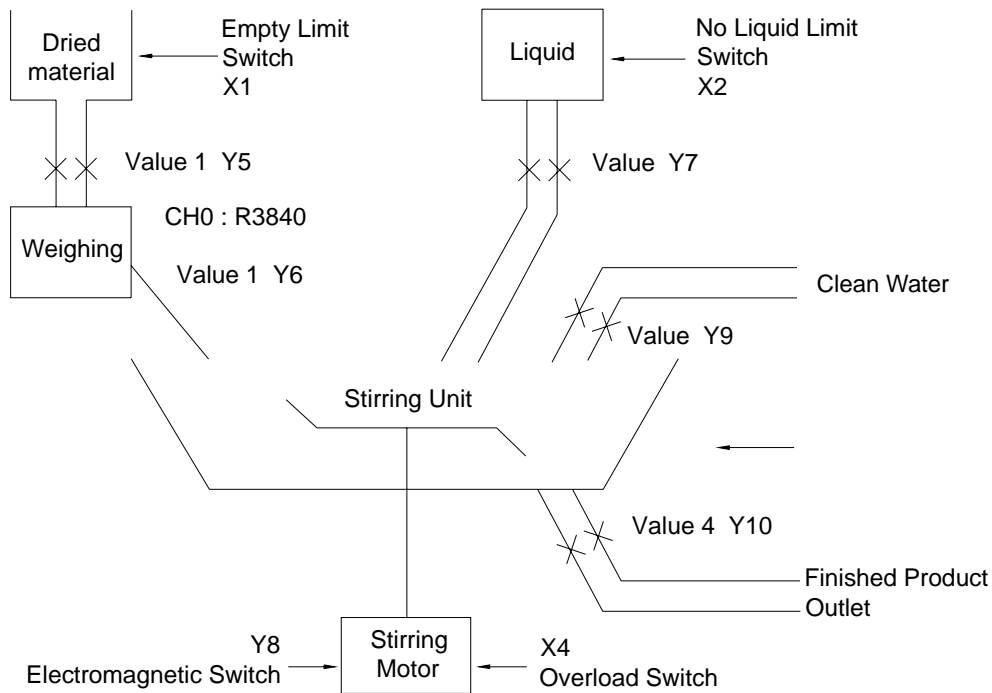
Divergent into S0 after moving to the left limit (a complete cycle)

```

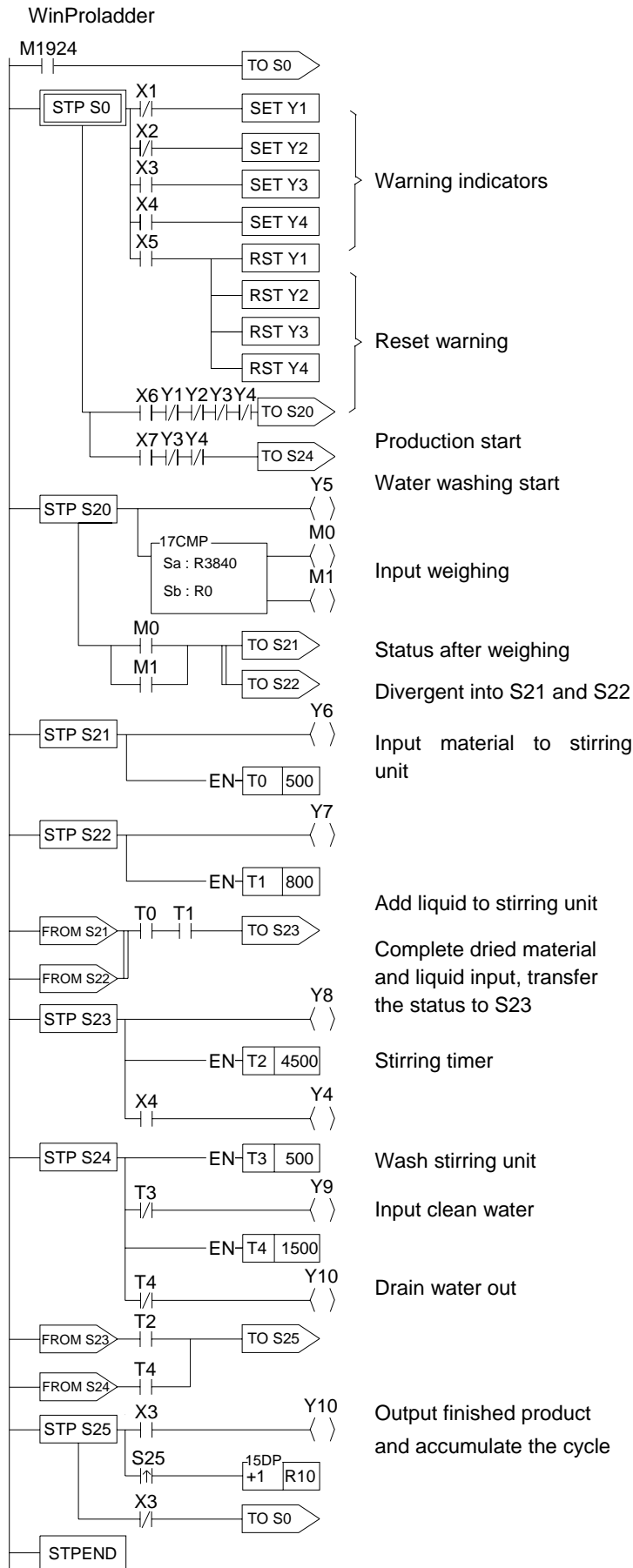
ORG      M1924
TO       S0
STP      S0
OUT TR   0
OUT NOT  Y4
AND NOT  X1
OUT      Y0
LD TR    0
AND NOT  X2
OUT      Y2
FROM     S0
AND      X0
TO       S20
STP      S20
OUT      Y3
FROM     S20
AND      X3
TO       S21
STP      S21
SET      Y4
T0 PV:   100
FROM     S21
AND      T0
TO       S22
STP      S22
OUT      Y2
FROM     S22
AND      X2
TO       S23
STP      S23
OUT      Y1
FROM     S23
AND      X4
TO       S24
STP      S24
OUT      Y3
FROM     S24
AND      X3
TO       S25
STP      S25
RST      Y4
T1 PV:   100
FROM     S25
AND      T1
TO       S26
STP      S26
OUT      Y2
FROM     S26
AND      X2
TO       S27
STP      S27
OUT      Y0
FROM     S27
AND      X1
TO       S0
STPEND

```

Example 2 Liquid Stirring Process



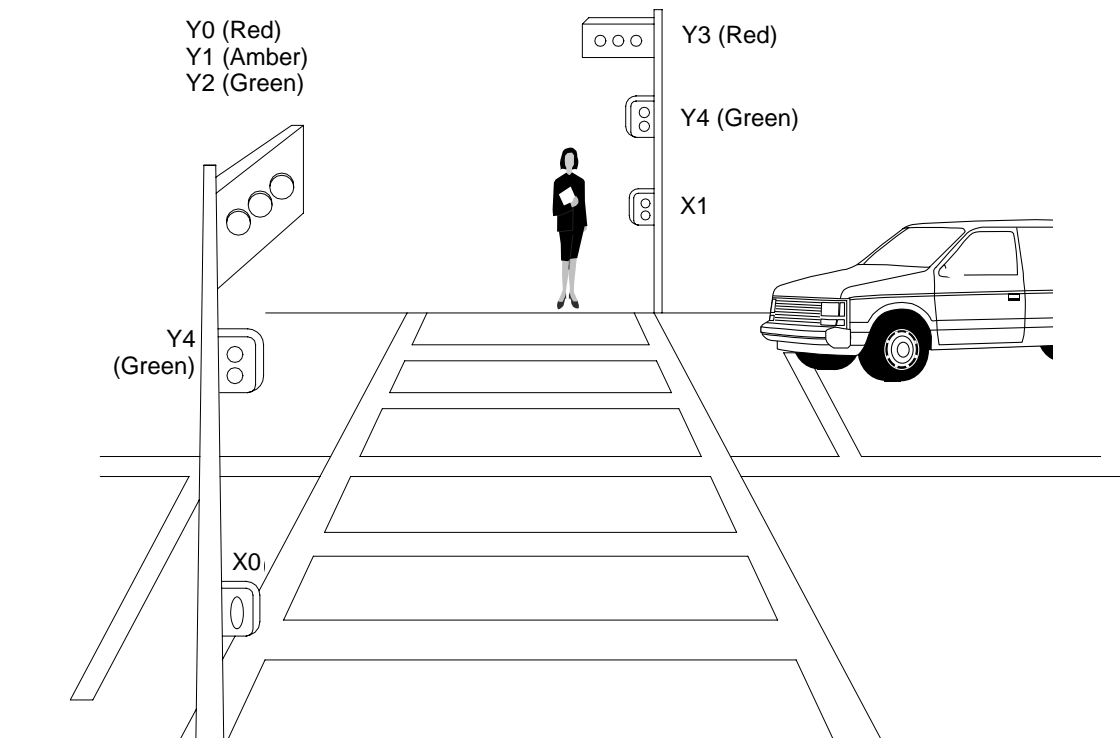
- **Input Points:** Empty limit switch X1
No liquid limit switch X2
Empty limit switch X3
Over-load switch X4
Warning clear button X5
Start button X6
Water washing button X7
- **Warning Indicators:** Empty dried material Y1
Insufficient liquid Y2
Empty stirring unit Y3
Motor over-load Y4
- **Output Points:** Dried material inlet valve Y5
Dried material inlet valve Y6
Liquid inlet valve Y7
Motor start electromagnetic valve Y8
Clean water inlet valve Y9
Finished product outlet valve Y10
- **Weighing Output:** CH0 (R3840)
- M1918=0



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ORG	M1924	STP	S22
TO	S0	OUT	Y7
STP	S0	T1 PV: 800	
OUT TR	0	FROM	S21
AND NOT	X1	FROM	S22
SET	Y1	AND	T0
LD TR	0	AND	T1
AND NOT	X2	TO	S23
SET	Y2	STP	S23
LD TR	0	OUT TR	0
AND	X3	OUT	Y8
SET	Y3	LD TR	0
LD TR	0	T2 PV: 4500	
AND	X4	LD TR	0
SET	Y4	AND	X4
LD TR	0	OUT	Y4
AND	X5	STP	S24
RST	Y1	OUT TR	0
RST	Y2	T3 PV: 500	
RST	Y3	LD TR	0
RST	Y4	AND NOT	T3
FROM	S0	OUT	Y9
OUT TR	1	LD TR	0
AND	X6	T4 PV: 1500	
AND NOT	Y1	LD TR	0
AND NOT	Y2	AND NOT	T4
AND NOT	Y3	OUT	Y10
AND NOT	Y4	FROM	S23
TO	S20	AND	T2
LD TR	1	FROM	S24
AND	X7	AND	T4
AND NOT	Y3	ORLD	
AND NOT	Y4	TO	S25
TO	S24	STP	S25
STP	S20	OUT TR	0
OUT	Y5	AND	X3
FUN	17	OUT	Y10
Sa:R3840 Sb:R0		LD TR	0
FO	0	AND TU	S25
OUT	M0	FUN	15DP
FO	1	D:R10	
OUT	M1	FROM	S25
FROM	S20	AND NOT	X3
LD	M0	TO	S0
OR	M1	STPEND	
ANDLD			
TO	S21		
TO	S22		
STP	S21		
OUT	Y6		
T0 PV: 500			

Example 3

Pedestrian Crossing Lights

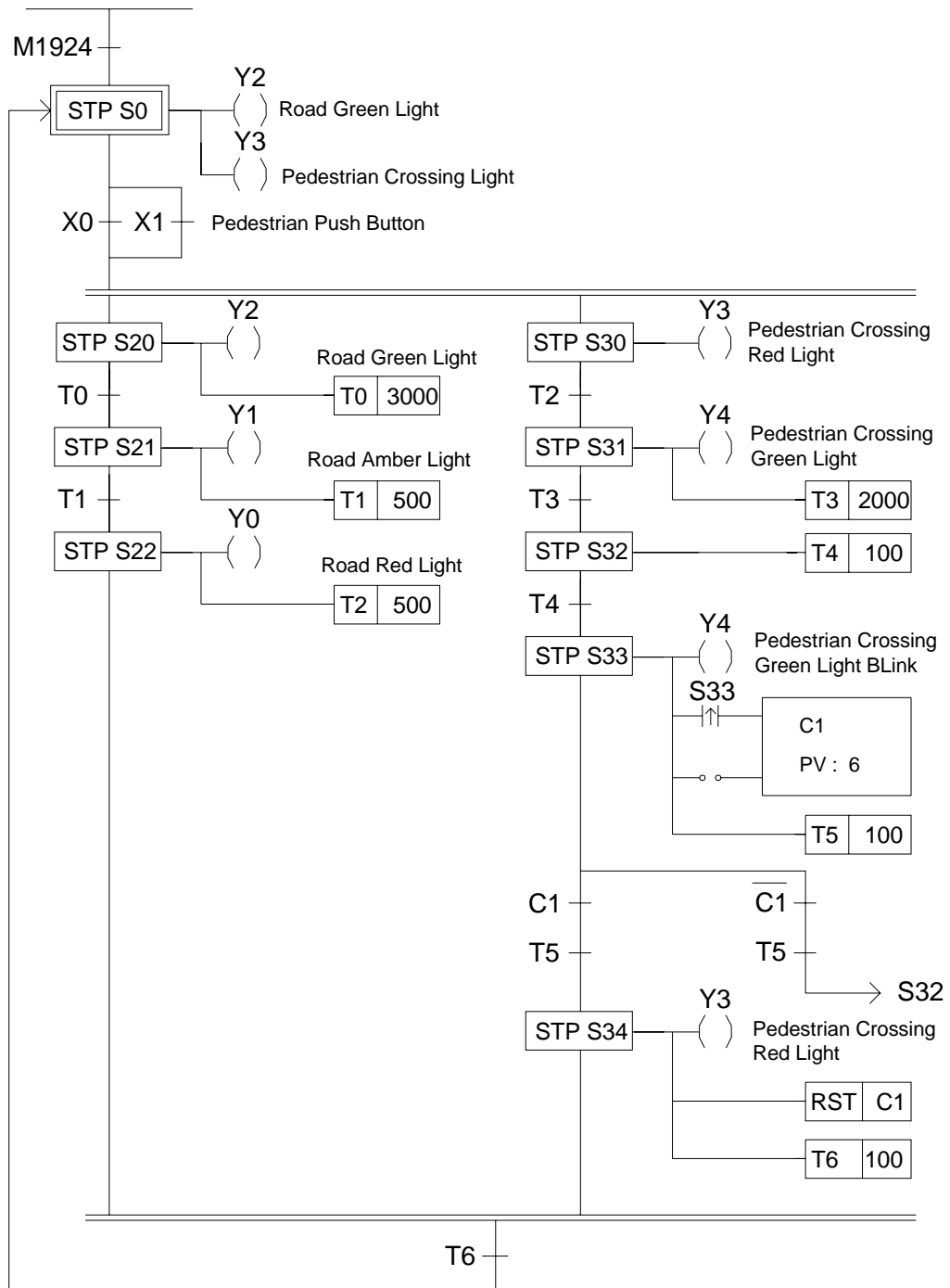


- ♦ Input Points: Pedestrian Push Button X0
Pedestrian Push Button X1

- ♦ Output Points: Road Red Light Y0
Road Amber light Y1
Road Green Light Y2
Pedestrian Crossing Red Light Y3
Pedestrian Crossing Green Light Y4

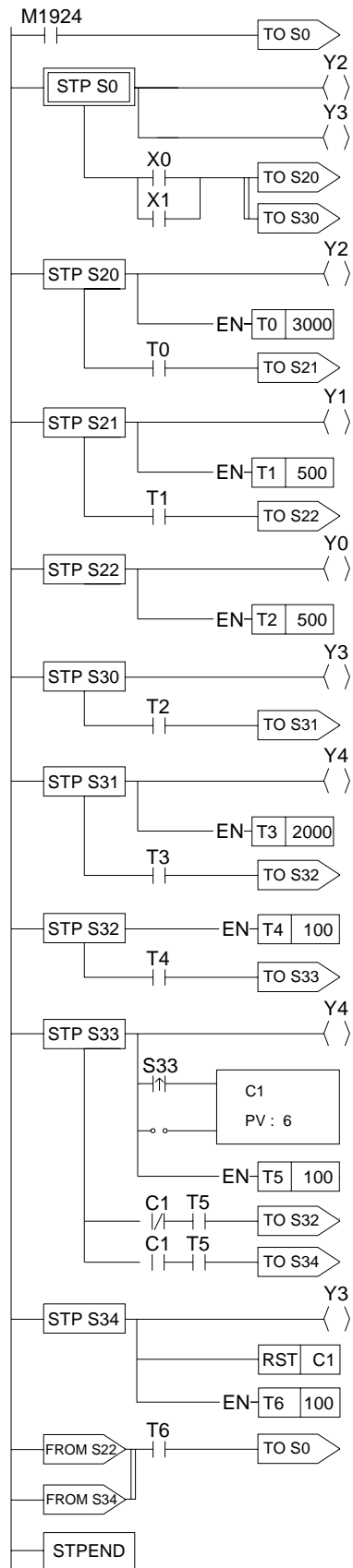
- ♦ M1918=0

● Pedestrian Crossing Lights Control Process Diagram



●

WinProladder



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ORG	M1924	STP	S32
TO	S0	T4 PV:	100
<hr/>			
STP	S0	FROM	S32
OUT	Y2	AND	T4
OUT	Y3	TO	S33
<hr/>			
FROM	S0	STP	S33
LD	X0	OUT TR	0
OR	X1	OUT	Y4
ANDLD		LD TR	0
TO	S20	AND TU	S33
TO	S30	LD	OPEN
<hr/>			
STP	S20	C1 PV:	6
OUT	Y2	LD TR	0
T0 PV:	3000	T5 PV:	100
FROM	S20	FROM	S33
AND	T0	OUT TR	1
TO	S21	AND NOT	C1
<hr/>			
STP	S21	AND	T5
OUT	Y1	TO	S32
T1 PV:	500	LD TR	1
FROM	S21	AND	C1
AND	T1	AND	T5
TO	S22	TO	S34
<hr/>			
STP	S22	STP	S34
OUT	Y0	OUT	Y3
T2 PV:	500	RST	C1
<hr/>			
STP	S30	T6 PV:	100
OUT	Y3	FROM	S22
FROM	S30	FROM	S34
AND	T2	AND	T6
TO	S31	TO	S0
<hr/>			
STP	S31	STPEND	
OUT	Y4		
T3 PV:	2000		
FROM	S31		
AND	T3		
TO	S32		

8.6 Syntax Check Error Codes for Step Instruction

The error codes for the usage of step instruction are as follows:

- E51 : TO(S0-S7) must begin with ORG instruction.
- E52 : TO(S20-S999) can't begin with ORG instruction.
- E53 : TO instruction without matched FROM instruction.
- E54 : To instruction must comes after TO, AND, OR, ANDLD or ORLD instruction.
- E56 : The instructions before FROM must be AND, OR, ANDLD or ORLD
- E57 : The instruction after FROM can't be a coil or a function
- E58 : Coil or function must before FROM while in STEP network
- E59 : More than 8 TO# at same network.
- E60 : More than 8 FROM# at same network.
- E61 : TO(S0-S19) must locate at first row of the network.
- E62 : A contact occupies the location for TO instruction.
- E72 : Duplicated TO Sxx instruction.
- E73 : Duplicated STP sxx instruction.
- E74 : Duplicated FROM sxx instruction.
- E76 : STP(S0~S19) without a matched STPEND or STPEND without a matched STP(S0~S19).
- E78 : TO(S20~S999), STP (S20~S999) or FROM instructions comes before or without STP(S0~S19).
- E79 : STP Sxx or FROM Sxx instructions comes before or without TO Sxx.
- E80 : FROM Sxx instruction comes before or without STP Sxx.
- E81 : The max. level of branches must ≤ 16 .
- E82 : The max. no. of branches with same level must ≤ 16 .
- E83 : Not place the step instruction with TO->STP->FROM sequence.
- E84 : The definition of STP# sequence not follow the TO# sequence.
- E85 : Convergence do not match the corresponding divergence.
- E86 : Illegal usage of STP or FROM before convergent with TO instruction.
- E87 : STP# or FROM# comes before corresponding TO#.
- E88 : During this branch, STP# or FROM# comes before the corresponding TO#.
- E89 : FROM# comes before corresponding TO# or STP#.
- E90 : Invalid To# usage in the simultaneous branch.
- E91 : Flow control function cannot be used in the step ladder region

Appendix I FBs-PACK Operation Instruction

The main unit of FBs series PLC provides the function to write ladder program and the selected data registers into MEMORY_PACK directly.

FBs-PACK is the product name of MEMORY PACK; the memory capacity is 64K WORD. Setting the DIP switch of the MEMORY_PACK at the unprotect position while writing, and at the protect ON position to avoid accidental writing.

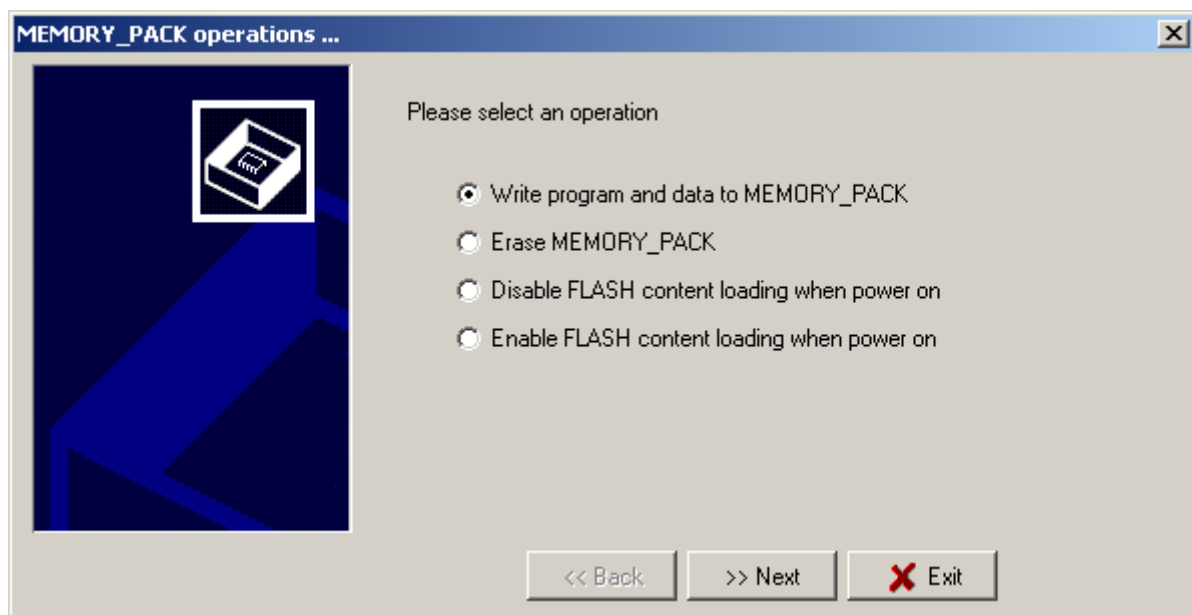
To operate friendly, WinProladder supports the corresponding MEMORY PACK operation interface; but for general usage, the direct register's access method is also introduced for further reference.

1.1 Write Program and Register Data to FBs-PACK Through WinProladder

Select Run MEMORY_PACK from Tool :

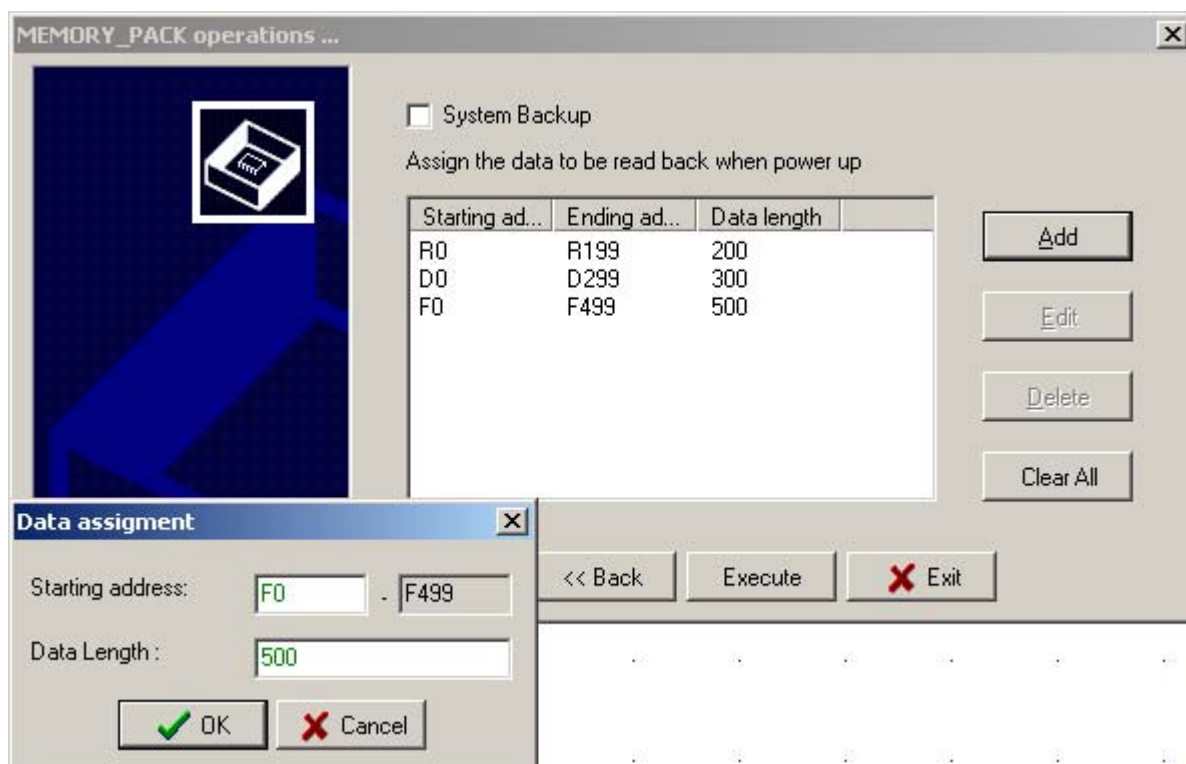
Tool

MEMORY_PACK operations :



- Write program and data to MEMORY_PACK :

Users can write programs and data into the MEMORY_PACK with this function. After clicking Next, the window display below :



Users can assign the range of registers which you want to read from MEMORY_PACK and write into PLC. If you don't want to back-up any data of register, press "Execute" to start. The execution time may differ depending on the size of ladder program and register data. During writing data into MEMORY_PACK, the system will appear the message "Under programming, please wait...". If the data are successfully stored into MEMORY_PACK, the message "MEMORY_PACK write OK" will appear. If it failed, the message "MEMORY_PACK write error" will appear.

- ※ It is allowed up to 4 groups of register or system backup for MEMORY_PACK manipulation, click "Add" or "Edit" or "Delete" to accomplish the writing and further retrieve of the selected registers.
- ※ The item "System Backup" means stored all of data (including the PLCID and station number of PLC) into MEMORY_PACK.

- System backup

There are two kinds of system backup for ROM PACK writing as below:

- ◆ System backup with PLC ID
- ◆ System backup without PLC ID

- While selecting the "System backup with PLC ID" for ROM PACK writing, the PLC main unit will read the PLC ID and ladder program from ROM PACK every power up if the ROM PACK has been installed for working; but all data registers and discrete status will read only once (Selecting "After initial system, read back the data one time") or every time (Selecting "When power on, read back the data every time") depending on the selective item.

It can make the ID (PLC ID and PROGRAM ID) copy for the main unit needing ID protection through this kind of ROM PACK without the intervention of programming tools.

This kind of ROM PACK can't be installed for working to have intellectual ID protection.

- While selecting the “System backup without PLC ID” for ROM PACK writing, the PLC main unit will read the ladder program from ROM PACK every power up if the ROM PACK has been installed for working; but all data registers and discrete status will read only once (Selecting “After initial system, read back the data one time”) or every time (Selecting “When power on, read back the data every time”) depending on the selective item.

It needs to have correct PLC ID setting for the PLC main unit to enter RUN mode if being installed ROM PACK with program ID protection; it means the PLC ID of the main unit must be same with the program ID of the ROM PACK, then the PLC main unit can work without problem.

This kind of ROM PACK can be installed for working to have intellectual ID protection; it is very suitable for mass production and long term maintenance with intellectual property protection.

- ※ While changing the PLC ID, the PLC ID will be written into the internal system FLASH ROM once at the next power up; it will keep the ID information even battery low.
- ※ While executing system initialization, the PLC ID will be erased from the internal system FLASH ROM once at the next power up if it exists.
- ※ While writing the ROM PACK with system backup, the motion parameter table (Assigned by FUN141) will also be included; it means the motion parameters will remain the settings even the system initialization being executed
- ※ It can support “Only read one time” function for ROM PACK accessing while writing the ROM PACK and selecting the item “After initial system, read back the data one time” for both data backup or system backup.

- Data Registers read PLC settings

- ※ “After initial system, read back the data one time” : the PLC main unit will read the data register and discrete status from the ROM PACK only one time at the first power up, and then the main unit doesn’t read the data register and discrete status again from the ROM PACK at the following power up. It is very useful to have default settings for the data registers from the ROM PACK, and after the default initialization, the data register can remain the new setting without loss at the next power up.
- ※ “When power on, read back the data every time” : the PLC main unit will read the data register and discrete status from the ROM PACK every power up. It is very useful to have the default settings for the data registers from the ROM PACK at every power up, the PLC main unit being equipped with this kind of ROM PACK can work properly even the battery low.

1.1.2 Erase MEMORY_PACK

Users can clear programs or data stored in MEMORY_PACK with this function. Click “NEXT”, it is showing “Under erase, please wait...”. It will show “MEMORY_PACK erase OK” if this erase is successful. It will show “MEMORY_PACK erase error” if this erase is failed.

1.1.3 Disable FLASH Content Loading When Power On:

Users can enter the test run modification mode with this function. Please Next to enter test run modification mode (Disable programs and data overwrite).

- ※ If the user needs to equip with a new MEMORY_PACK, selecting this item first to avoid the undesired overwrite of ladder program by which storing in the new MEMORY_PACK while power up. This function is used to let the main unit enter into the “Modify and Testing” mode for programming if it equips with the MEMORY_PACK. Please refer to the next page for detailed description.

1.1.4 Enable FLASH Content Loading When Power On:

Please Next to complete normal mode setup.

- ※ Every power up, the ladder program and the selected data registers storing in battery backup RAM of the main unit will be placed by which storing in the MEMORY_PACK (if this MEMORY_PACK was equipped with the main unit and it had ever been written the ladder program), and the PLC will enter into “RUN” mode automatically regardless it’s “RUN” or “STOP” mode before.

1.2 Write Program and Register Data to FBs-PACK Through Special Register Operation

To meet the application needs of different customers, users can write data into MEMORY_PACK by setting special register. WinProladder users can skip this section because setting actions will be completed at the same time when executing MEMORY_PACK options with WinProladder.

Operation relevant special register

- R4052 : Dedicated register for MEMORY_PACK operation.

Register	Content value	Functions
R4052	5530H (Test run modification mode)	<p>Modify & Test mode for PLC programming while main unit being equipped with the MEMORY_PACK.</p> <p>There are 2 kinds of memory on main unit to store the ladder program and data registers; one is the battery backup RAM, this is standard equipment and the ladder program and data registers must be executed here; another memory to store the ladder program and data registers is the optional MEMORY_PACK, the ladder program and data registers can't be executed here directly. In Modify & Test mode, the ladder program and data registers storing in battery backup RAM of main unit will not be overwritten by the MEMORY_PACK's while power up; it means the content of the battery backup RAM will be kept, and the modification if ever will not be lost, this is so called "Modify & Test mode".</p> <p>After the modification and testing has been finished, writing the ladder program and data registers into the MEMORY_PACK is a better way for long term saving and easy after sale service of maintenance or for mass</p>

R4052		copy of same machine's program. During the modification and testing, if the user want to give up the change, it is only to set R4052 to be 0, and turn off then turn on the power again, the ladder program and data registers storing in battery backup RAM will be overwritten by which storing in the MEMORY_PACK while power up, the main unit will return to the environment before modification.
	Other value	Normal operation or Writing mode. If the main unit equips with the optional MEMORY_PACK, and the MEMORY_PACK had ever been written the ladder program before, while every power up, the ladder program storing in battery backup RAM of the main unit will be replaced by which storing in the MEMORY_PACK, and the PLC will enter into "RUN" mode automatically regardless it's "RUN" or "STOP" mode before.

- R4046 : Dedicated register to retrieve the data registers storing in ROM_PACK.

While writing the ladder program into the MEMORY_PACK along with the selected data registers, the content of the selected data registers (locating at the RAM of the main unit) will be initialized with the values which previously being written into the MEMORY_PACK on each power up; it is very useful for machine turning parameter's long term saving and after sale service of maintenance.

But in many applications, it needs only one time initialization for the selected data registers while the first power up and then the contents of those will be retentive after followings' power up.

User may control the value of R4046 to accomplish above mentioned applications.

Register	Content value	Functions
R4046	5530H	The selected data registers of the main unit will not be initialized with the values which previously being written into the MEMORY_PACK while power up.
	Other value	The selected data registers of the main unit will be initialized with the values which previously being written into the MEMORY_PACK while power up.

- ※ If it needs only one time initialization for selected data registers while the first power up, fill the register R4046 with the value 5530H in the ladder program.

- Either PLC in RUN or in STOP mode, the user can give the command to clear MEMORY_PACK or write the ladder program and selected registers into MEMORY_PACK.

Register	Content value	Functions
	5550H	giving the command to clear MEMORY_PACK
	5551H	the status to say " Being cleared"
	5552H	the status to say "Verify for clearing"
	5553H	the status to say "Complete the clear command "
	5554H	the status to say "Failed to clear the MEMORY_PACK"
	5560H	giving the command to write ladder program and selected registers into MEMORY_PACK

R4052	5562H	the status to say "Writing the Ladder Program"
	5563H	the status to say "Writing the Registers"
	5566H	the status to say "Verify the Ladder Program"
	5567H	the status to say "Verify the Registers"
	556AH	the status to say "Complete the writing"
	556BH	the status to say "Failed to write ladder program"
	556CH	the status to say "Failed to write registers"

1.3 Assigning the Retrieval of Register Stored FBs-PACK

- The contents of the selected registers can be written into the MEMORY_PACK and those will be read back from the MEMORY_PACK for initialization while every power up. The turning values or fixed preset values can be written into the MEMORY_PACK for this kind of application to keep proper operation even the loss of the battery power.
- The special registers of R4030~R4039 are used to assign which group of registers needed to be written into MEMORY_PACK for above mentioned application, it is necessary to do the assignment first before giving command to write the MEMORY_PACK.

Register	Content value	Functions
R4030	A66AH	It is the identification flag to tell the selected registers needed be written into and read back from the MEMORY_PACK according to the following settings of R4031~R4039 (Retentive registers support this function).
	Other value	There is not any register needed be written into and read back from the MEMORY_PACK.
R4031	1~4	Quantity of register groups needed be written into and read back from the MEMORY_PACK (4 in maximum).
R4032	Length 0	The data length of register group 0. The length is between 1 ~ 3840 for register R0 ~ R3839; The length is between 1 ~ 3072 for register R5000 ~ R8071; The length is between 1 ~ 4096 for register D0 ~ D4095; The length is between 1 ~ 166 for register R4000 ~ R4165; While the length is 7FF7H, it means for system backup including the PLC ID and station number of PLC ; It will not work when illegal length or out of range;
R4033	Start 0	The starting address of register group 0. The address is between 0 ~ 3839 for register R0 ~ R3839; The address is between 5000 ~ 8071 for R5000 ~ R8071; The address is between 10000 ~ 14095 for D0 ~ D4095; (The address must be added by 10000 for register Dxxxx) The address is between 4000 ~ 4165 for R4000 ~ R4165; R4033 and R4032 are used in pair.

R4034	Length 1	The data length of register group 1. The ranges of length same as mentioned above for R4032;
R4035	Start 1	The starting address of of register group 1. The ranges of address same as mentioned above for R4033; R4035 and R4034 are used in pair.
R4036	Length 2	The data length of register group 2 The ranges of length same as mentioned above for R4032;
R4037	Start 2	the starting address of of register group 2 The ranges of address same as mentioned above for R4033; R4037 and R4036 are used in pair.
Register	Content value	Functions
R4038	Length 3	The data length of register group 3 The ranges of length same as mentioned above for R4032;
R4039	Start 3	the starting address of of register group 3 The ranges of address same as mentioned above for R4033; R4039 and R4038 are used in pair.

1.4 Read and Write FBs-PACK by Function Instruction

You also can read and write data or ladder program by Function Instruction(FUN161 、FUN162). Please refer to 7-144 ~ 7-147 for the instructions explanation and program example for FUN161 and FUN162.